FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-30326-1E

*MEMORY*

# FLASH MEMORY CARD
## PCMCIA Rel.2/JEIDA Ver.4 conformable

# MB98A8113x-/8123x-/8133x-/8143x-20



**FLASH ERASABLE AND PROGRAMMABLE MEMORY CARD**
**2 M/4 M/8 M/16 M-BYTE**

## ■ DESCRIPTION

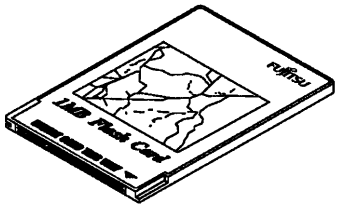
The Fujitsu MB98A8113x, MB98A8123x, MB98A8133x and MB98A8143x are electrically erasable and programmable (Flash) memory cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuit is protected by two metal panels, one at the top and the other at the bottom of the card, that help to reduce chip damage from electrostatic discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card Internal Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specifications, Flash memory cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is a Flash memory card option. (See page 2 for description of the three available options.)

- Conformed to PCMCIA and JEIDA industry standards.
- Credit card size: 85.6 mm (length) × 54.0 mm (width) × 3.3 mm (thickness)
- PCMCIA/JEIDA conformed two-piece 68-pin connector (with a two-row built-in receptacle)
- Single +5 V ±5% power supply (+12.0 V ±5%$V_{PP}$)
- Command control for Automated Program/Automated Erase operation
- Write protect function
- Erase Suspend Capability
- Status Resister Capability
- 128 KB Block Erase (at ×16 mode)

## ■ PACKAGE




(CRD-68P-M05)

# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by the customers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the $\overline{\text{REG}}$ pin on the card interface. Option descriptions as follows:

**OPTION 1: Attribute memory is not supported.**
**$\overline{\text{REG}}$ Pin: Not Contacted**

(JEIDA Ver. 3 conformable)

| Part Number | Main Memory | | Attribute Memory | | Memory Organization * |
|---|---|---|---|---|---|
| | Memory Device | Access Time | Memory Device | Access Time | |
| MB98A81131 | 8 M Flash Memory × 2 pcs | 200 ns | — | — | 2 M × 8 bits/1 M × 16 bits |
| MB98A81231 | 8 M Flash Memory × 4 pcs | 200 ns | — | — | 4 M × 8 bits/2 M × 16 bits |
| MB98A81331 | 8 M Flash Memory × 8 pcs | 200 ns | — | — | 8 M × 8 bits/4 M × 16 bits |
| MB98A81431 | 8 M Flash Memory × 16 pcs | 200 ns | — | — | 16 M × 8 bits/8 M × 16 bits |

**OPTION 2: Attribute memory in a separate location is not supported.**

**When $\overline{\text{REG}}$ line is asserted, "FF" is output to the data bus to indicate that attribute data may be stored in main memory.**

(PCMCIA Rel. 2/JEIDA Ver. 4 conformable)

| Part Number | Main Memory | | Attribute Memory | | Memory Organization * |
|---|---|---|---|---|---|
| | Memory Device | Access Time | Memory Device | Access Time | |
| MB98A81132 | 8 M Flash Memory × 2 pcs | 200 ns | — | — | 2 M × 8 bits/1 M × 16 bits |
| MB98A81232 | 8 M Flash Memory × 4 pcs | 200 ns | — | — | 4 M × 8 bits/2 M × 16 bits |
| MB98A81332 | 8 M Flash Memory × 8 pcs | 200 ns | — | — | 8 M × 8 bits/4 M × 16 bits |
| MB98A81432 | 8 M Flash Memory × 16 pcs | 200 ns | — | — | 16 M × 8 bits/8 M × 16 bits |

**OPTION 3: Attribute memory is supported. The data is stored in 64 K-bit EEPROM.**

**When the $\overline{\text{REG}}$ line is asserted, data stored in EEPROM is output to the data bus.**

(PCMCIA Rel. 2/JEIDA Ver. 4 conformable)

| Part Number | Main Memory | | Attribute Memory | | Memory Organization * |
|---|---|---|---|---|---|
| | Memory Device | Access Time | Memory Device | Access Time | |
| MB98A81133 | 8 M Flash Memory × 2 pcs | 200 ns | EEPROM × 1 pcs | 300 ns | 2 M × 8 bits/1 M × 16 bits |
| MB98A81233 | 8 M Flash Memory × 4 pcs | 200 ns | EEPROM × 1 pcs | 300 ns | 4 M × 8 bits/2 M × 16 bits |
| MB98A81333 | 8 M Flash Memory × 8 pcs | 200 ns | EEPROM × 1 pcs | 300 ns | 8 M × 8 bits/4 M × 16 bits |
| MB98A81433 | 8 M Flash Memory × 16 pcs | 200 ns | EEPROM × 1 pcs | 300 ns | 16 M × 8 bits/8 M × 16 bits |

* : To be configured by user.

# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ PIN ASSIGNMENTS

| MB98A8113x | MB98A8123x | MB98A8133x | MB98A8143x | Pin No. | | MB98A8113x | MB98A8123x | MB98A8133x | MB98A8143x |
|---|---|---|---|---|---|---|---|---|---|
| GND | GND | GND | GND | 1 | 35 | GND | GND | GND | GND |
| $D_3$ | $D_3$ | $D_3$ | $D_3$ | 2 | 36 | $\overline{CD_1}$ | $\overline{CD_1}$ | $\overline{CD_1}$ | $\overline{CD_1}$ |
| $D_4$ | $D_4$ | $D_4$ | $D_4$ | 3 | 37 | $D_{11}$ | $D_{11}$ | $D_{11}$ | $D_{11}$ |
| $D_5$ | $D_5$ | $D_5$ | $D_5$ | 4 | 38 | $D_{12}$ | $D_{12}$ | $D_{12}$ | $D_{12}$ |
| $D_6$ | $D_6$ | $D_6$ | $D_6$ | 5 | 39 | $D_{13}$ | $D_{13}$ | $D_{13}$ | $D_{13}$ |
| $D_7$ | $D_7$ | $D_7$ | $D_7$ | 6 | 40 | $D_{14}$ | $D_{14}$ | $D_{14}$ | $D_{14}$ |
| $\overline{CE_1}$ | $\overline{CE_1}$ | $\overline{CE_1}$ | $\overline{CE_1}$ | 7 | 41 | $D_{15}$ | $D_{15}$ | $D_{15}$ | $D_{15}$ |
| $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ | 8 | 42 | $\overline{CE_2}$ | $\overline{CE_2}$ | $\overline{CE_2}$ | $\overline{CE_2}$ |
| $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}$ | 9 | 43 | N.C. | N.C. | N.C. | N.C. |
| $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ | 10 | 44 | N.C. | N.C. | N.C. | N.C. |
| $A_9$ | $A_9$ | $A_9$ | $A_9$ | 11 | 45 | N.C. | N.C. | N.C. | N.C. |
| $A_8$ | $A_8$ | $A_8$ | $A_8$ | 12 | 46 | $A_{17}$ | $A_{17}$ | $A_{17}$ | $A_{17}$ |
| $A_{13}$ | $A_{13}$ | $A_{13}$ | $A_{13}$ | 13 | 47 | $A_{18}$ | $A_{18}$ | $A_{18}$ | $A_{18}$ |
| $A_{14}$ | $A_{14}$ | $A_{14}$ | $A_{14}$ | 14 | 48 | $A_{19}$ | $A_{19}$ | $A_{19}$ | $A_{19}$ |
| $\overline{WE}$ | $\overline{WE}$ | $\overline{WE}$ | $\overline{WE}$ | 15 | 49 | $A_{20}$ | $A_{20}$ | $A_{20}$ | $A_{20}$ |
| N.C. | N.C. | N.C. | N.C. | 16 | 50 | N.C. | $A_{21}$ | $A_{21}$ | $A_{21}$ |
| $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | 17 | 51 | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $V_{PP1}$ | $V_{PP1}$ | $V_{PP1}$ | $V_{PP1}$ | 18 | 52 | $V_{PP2}$ | $V_{PP2}$ | $V_{PP2}$ | $V_{PP2}$ |
| $A_{16}$ | $A_{16}$ | $A_{16}$ | $A_{16}$ | 19 | 53 | N.C. | N.C. | $A_{22}$ | $A_{22}$ |
| $A_{15}$ | $A_{15}$ | $A_{15}$ | $A_{15}$ | 20 | 54 | N.C. | N.C. | N.C. | $A_{23}$ |
| $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ | 21 | 55 | N.C. | N.C. | N.C. | N.C. |
| $A_7$ | $A_7$ | $A_7$ | $A_7$ | 22 | 56 | N.C. | N.C. | N.C. | N.C. |
| $A_6$ | $A_6$ | $A_6$ | $A_6$ | 23 | 57 | N.C. | N.C. | N.C. | N.C. |
| $A_5$ | $A_5$ | $A_5$ | $A_5$ | 24 | 58 | N.C. | N.C. | N.C. | N.C. |
| $A_4$ | $A_4$ | $A_4$ | $A_4$ | 25 | 59 | N.C. | N.C. | N.C. | N.C. |
| $A_3$ | $A_3$ | $A_3$ | $A_3$ | 26 | 60 | N.C. | N.C. | N.C. | N.C. |
| $A_2$ | $A_2$ | $A_2$ | $A_2$ | 27 | 61 | $\overline{REG}$/N.C.* | $\overline{REG}$/N.C.* | $\overline{REG}$/N.C.* | $\overline{REG}$/N.C.* |
| $A_1$ | $A_1$ | $A_1$ | $A_1$ | 28 | 62 | BVD2 | BVD2 | BVD2 | BVD2 |
| $A_0$ | $A_0$ | $A_0$ | $A_0$ | 29 | 63 | BVD1 | BVD1 | BVD1 | BVD1 |
| $D_0$ | $D_0$ | $D_0$ | $D_0$ | 30 | 64 | $D_8$ | $D_8$ | $D_8$ | $D_8$ |
| $D_1$ | $D_1$ | $D_1$ | $D_1$ | 31 | 65 | $D_9$ | $D_9$ | $D_9$ | $D_9$ |
| $D_2$ | $D_2$ | $D_2$ | $D_2$ | 32 | 66 | $D_{10}$ | $D_{10}$ | $D_{10}$ | $D_{10}$ |
| WP | WP | WP | WP | 33 | 67 | $\overline{CD_2}$ | $\overline{CD_2}$ | $\overline{CD_2}$ | $\overline{CD_2}$ |
| GND | GND | GND | GND | 34 | 68 | GND | GND | GND | GND |

* : N.C. terminal in MB98A8xx31 series.

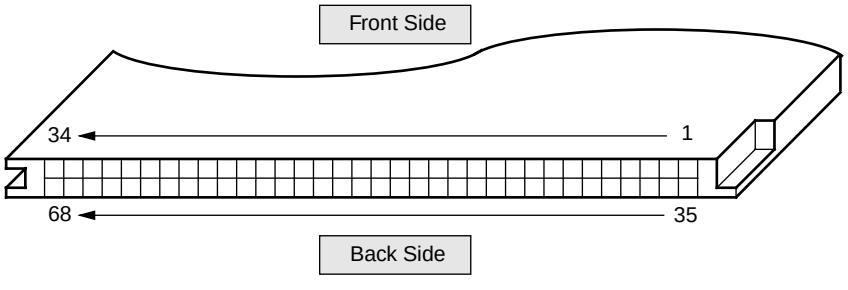
# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ PIN DESCRIPTIONS

| Symbol | Pin Name | Input/Output | Function |
|---|---|---|---|
| $A_0$ to $A_{23}$ | Address Input | Input | Address Inputs, $A_0$ to $A_{23}$. |
| $D_0$ to $D_{15}$ | Data Input/Output | Input/Output | Data Inputs/Outputs.<br>This data bus size (8-bit or 16-bit) is selected with $\overline{CE}_1$ and $\overline{CE}_2$. |
| $\overline{CE}_1$ | Card Enable for Lower Byte | Input | Active Low.<br>- Lower byte ($D_0$ to $D_7$) is selected for read/write/ erase function of flash memory cards. |
| $\overline{CE}_2$ | Card Enable for Upper Byte | Input | Active Low.<br>- Upper byte ($D_8$ to $D_{15}$) is selected for read/write / erase function of flash memory cards. |
| $\overline{REG}$ | Attribute Memory Select | Input | Active Low.<br>- Attribute memory is selected for read/write function of identification data of flash memory cards. (N.C. or “FF” data or attribute data.) |
| $\overline{OE}$ | Output Enable | Input | Active Low.<br>- Output enable for flash memory cards. |
| $\overline{WE}$ | Write Enable | Input | Active Low.<br>- Write enable for flash memory cards. |
| $V_{PP1}$ | Programming Voltage 1 | Input | Programming voltage for lower byte. |
| $V_{PP2}$ | Programming Voltage 2 | Input | Programming voltage for upper byte. |
| $\overline{CD}_1$, $\overline{CD}_2$ | Card Detect | Output | These pins detect if the card has been correctly inserted. Both pins are tied to GND internally. |
| WP | Write Protect | Output | Write controller for flash memory cards.<br>This pin outputs the Protect/Non Protect status of “WP Switch”. |
| BVD1, BVD2 | Battery Voltage Detect | Output | Both pins are tied to $V_{CC}$ internally. |
| $V_{CC}$ | Power Supply | — | Power Supply Voltage. (+5.0 V ±5%) |
| GND | Ground | — | System Ground. |
| N.C. | Non Connection | — | |

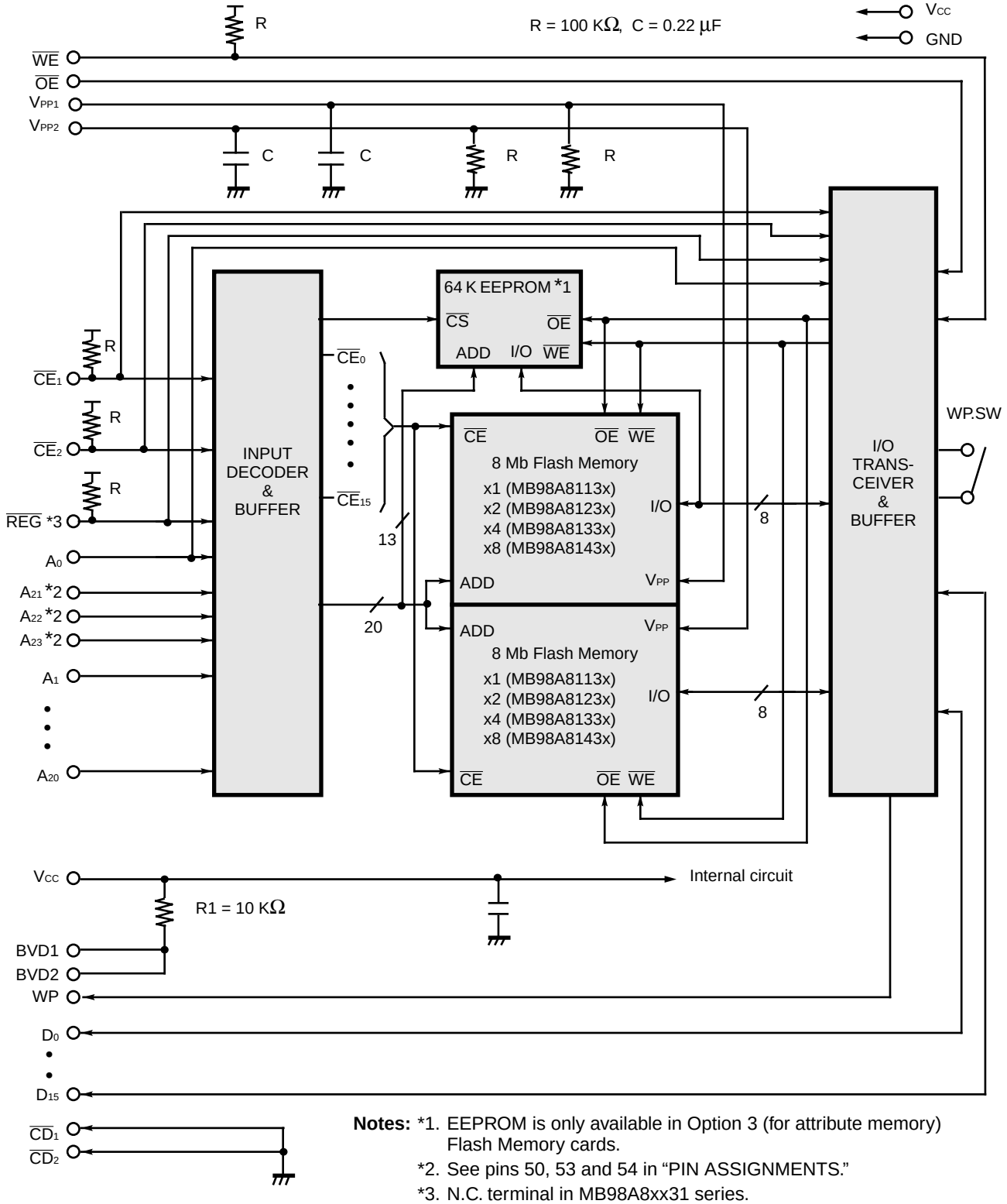
## ■ PIN LOCATIONS

**Fig. 1 – BOTTOM VIEW (CONNECTOR SIDE)**



# MB98A8113x-/8123x-/8133x-/8143x-20

**Fig. 2 – MB98A8113x, 8123x, 8133x, and 8143x BLOCK DIAGRAM**




**Notes:** *1. EEPROM is only available in Option 3 (for attribute memory) Flash Memory cards.

*2. See pins 50, 53 and 54 in “PIN ASSIGNMENTS.”

*3. N.C. terminal in MB98A8xx31 series.

## ■ FUNCTION DESCRIPTIONS

MB98A8113x, 8123x, 8133x and 8143x have the common memory and the attribute one, and $\overline{REG}$ selects the common memory ($\overline{REG}$ = $V_{IH}$) or the attribute memory ($\overline{REG}$ = $V_{IL}$).

MB98A8xx31 has the common memory only and $\overline{REG}$ pin is non-connected. If the attribute data is necessary, the data is programmed into the common memory. MB98A8xx32 has also the common memory only and "FFH" is output if the attribute data is read. MB98A8xx33 has both common memory and attribute memory.

### 1. Read Mode

The data in the common and attribute memory can be read with "$\overline{OE}$ = $V_{IL}$" and "$\overline{WE}$ = $V_{IH}$". The address is selected with $A_0$ to $A_{23}$. And $\overline{CE}_1$ and $\overline{CE}_2$ select output mode (×8/×16 output mode).
The following 1) and 2) are the descriptions for Common Memory Read and Attribute Memory Read mode.

1) Common Memory Read
   – Three modes of Common Memory Read, reading the data in memory array, Intelligent ID and Status Register, are available. The card entered each Read Mode by writing "Read Memory/Reset Command", "Intelligent ID Read Command" or "Status Register Read Command". At writing each command, $V_{PP}$ is "$V_{PPL}$" or "$V_{PPH}$". The card automatically resets to the condition of Common Memory Read Mode upon initial power-up.

2) Attribute Memory Read
   – The data on the attribute memory can be read with "$\overline{REG}$ = $V_{IL}$", "$\overline{OE}$ = $V_{IL}$" and "$\overline{WE}$ = $V_{IH}$".
   – An address on attribute memory can be selected with $A_0$ to $A_{13}$ pin. And $\overline{CE}_1$ and $\overline{CE}_2$ select output mode.

### 2. Standby Mode

– $\overline{CE}_1$ and $\overline{CE}_2$ at "$V_{IH}$" place the card in Standby mode. $D_0$ to $D_{15}$ are placed in a high-Z state independent of the status "$\overline{OE}$", "$\overline{WE}$" and "$\overline{REG}$".

### 3. Output Disable Mode

– The outputs are disabled with $\overline{OE}$ and $\overline{WE}$ at "$V_{IH}$". $D_0$ to $D_{15}$ are placed in high-Z state.

### 4. Write Mode

1) Common Memory Write
   – The card is in Write mode with "$\overline{OE}$ = $V_{IH}$" and "$\overline{WE}$ and $\overline{CE}$ = $V_{IL}$". Commands can be written at the write mode.
   – $V_{PP}$ must be placed in "$V_{PPH}$" at programming and erase operations only. And "$V_{PP}$ = $V_{PPL}$ or $V_{PPH}$" at other write mode. Two types of the write mode, "$\overline{WE}$ control" and "$\overline{CE}$ control" are available.

2) Attribute Memory Write
   – $\overline{REG}$ at L-level selects Attribute memory and "$\overline{OE}$ = $V_{IH}$", "$\overline{WE}$ and $\overline{CE}$ = $V_{IL}$" place it in write mode. Two types of the write mode, "$\overline{WE}$ control" and "$\overline{CE}$ control" are available.
   – Attribute memory is not controlled by writing Commands. And attribute memory has the data polling function, which can detect whether the card status is programming operation. If the read operation is executed at programming cycle, the opposite data ($\overline{I_7}$) to written data is output from $D_7$ pin at the programming operation, and the same data ($O_7$) as the written data is output from $D_7$ pin at the completion of programming operation.

### 5. Automated Program Capability

– The card automatically executes the operation from programming to verification by one time of writing "Setup Program/Program command".
– Address and data are latched at rising edge of $\overline{WE}$ or $\overline{CE}$.
– The card contains a Status Register which is read to check whether a byte (word) programming operation is completed successfully.
– If $V_{PP}$ goes "$V_{PPL}$" at programming operation, VPPS of Status Register does not indicate "1", but a result of the programming is not guaranteed. In this case, there is a possibility that the incorrect data are written and therefore, the written data should be erased to be reprogrammed.

### 6. Automated Erase Capability

– The card automatically executes the operation from erasing to verification by one time of writing “Setup erase/ erase command”.
– Address and data are latched at rising edge of “WE” or “CE”.
– Whether or not block erase operation is completed successfully can be checked by reading Status Register.
– If $V_{PP}$ goes “$V_{PPL}$” at erase operation, VPPS of Status Register does not indicate “1”, but a result of the erase is not guaranteed. Therefore, erase should be executed once again.

### 7. Status Register

– The card contains a Status Register for each chip to show the status of the common memory.
– Status Register is automatically read after Status Register Read command, Program command, Erase command, Erase Resume command or Erase Suspend command is input. After writing this command, all subsequent read operations output data from the status register until another valid command is written.
– The contents of Status Register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last in the cycle. $\overline{OE}$ or $\overline{CE}$ must be toggled to $V_{IH}$ before further reads to update the Status Register latch.
– The Read Status Register command functions when $V_{PP} = V_{PPL}$ or $V_{PPH}$.

### 8. Erase Suspend

– The Erase Suspend Command allows block erase interruption in order to read data from another block of memory.
– By writing the Erase Suspend Command (B0H) to chip in erasing state, the Write State Machine (WSM) suspends the erase sequence in the erase algorithm. At this point, a Read Command (FFH) can be written to read the data from block other than that suspended.
– Other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H). By writing the Erase Resume Command into the chip with suspended block, the WSM will execute the erase process again.
– $V_{PP}$ must remain at $V_{PPH}$ while the card is in Erase Suspend.
– The Erase Suspend status can be checked by Status Register Read. When Erase Suspend Status (ESS) bit of Status Register is “1”, the card is in the Suspend Status. At erase operation, “0” is output from Write State Machine Status (WSMS) bit. At erase suspend status, “1” is output from WSMS.

### 9. Intelligent Identifier (ID) Read Mode

– Each common memory can execute an intelligent identifier operation, initiated by writing Intelligent ID command (90H). Following the command write, a read cycle from address 00H retrieves the manufacture code of 89H, and a read cycle from address 01H returns the device code of A2H. To terminate the operation, it is necessary to write another valid command.
– The intelligent ID command is functional when $V_{PP} = V_{PPL}$ or $V_{PPH}$.

# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ FUNCTIONAL TRUTH TABLE

### MAIN MEMORY FUNCTION *1

**Read Function ($\overline{REG}$ = $V_{IH}$)**

| $\overline{CE}_2$ | $\overline{CE}_1$ | $A_0$ | $\overline{OE}$ | $\overline{WE}$ | WP *2 | $V_{PP2}$ | $V_{PP1}$ | Mode | Data Input/Output | | WP SW |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | $D_8$ to $D_{15}$ | $D_0$ to $D_7$ | |
| H | H | X | X | X | X | $V_{PPX}$ | $V_{PPX}$ | Standby | High-Z | | P or NP |
| H | L | L | L | H | X | $V_{PPX}$ | $V_{PPX}$ | Read (×8 No.1) | High-Z | $D_{OUT}$ (Lower Byte) | P or NP |
| H | L | H | L | H | X | $V_{PPX}$ | $V_{PPX}$ | Read (×8 No.1) | High-Z | $D_{OUT}$ (Upper Byte) | P or NP |
| L | H | X | L | H | X | $V_{PPX}$ | $V_{PPX}$ | Read (×8 No.2) | $D_{OUT}$ (Upper Byte) | High-Z | P or NP |
| L | L | X | L | H | X | $V_{PPX}$ | $V_{PPX}$ | Read (×16) | $D_{OUT}$ | | P or NP |
| X | X | X | H | H | X | $V_{PPX}$ | $V_{PPX}$ | Output Disable | High-Z | | P or NP |

**Write Command/Erase/Program Function ($\overline{REG}$ = $V_{IH}$)**

| $\overline{CE}_2$ | $\overline{CE}_1$ | $A_0$ | $\overline{OE}$ | $\overline{WE}$ | WP *2 | $V_{PP2}$ | $V_{PP1}$ | Mode | Data Input/Output | | WP SW |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | $D_8$ to $D_{15}$ | $D_0$ to $D_7$ | |
| H | H | X | X | X | X | $V_{PPX}$ *3 | $V_{PPX}$ *3 | Standby | High-Z | | P or NP |
| H | L | L | L | H | X | $V_{PPX}$ | $V_{PPX}$ *3 | Read (×8 No.1) | High-Z | $D_{OUT}$ (Lower Byte) | P or NP |
| H | L | H | L | H | X | $V_{PPX}$ *3 | $V_{PPX}$ | Read (×8 No.1) | High-Z | $D_{OUT}$ (Upper Byte) | P or NP |
| H | L | L | H | L | L | $V_{PPX}$ | $V_{PPX}$ *3 | Write (×8 No.1) | High-Z | $D_{IN}$ (Lower Byte) | NP |
| H | L | H | H | L | L | $V_{PPX}$ *3 | $V_{PPX}$ | Write (×8 No.1) | High-Z | $D_{IN}$ (Upper Byte) | NP |
| L | H | X | L | H | X | $V_{PPX}$ *3 | $V_{PPX}$ | Read (×8 No.2) | $D_{OUT}$ (Upper Byte) | High-Z | P or NP |
| L | H | X | H | L | L | $V_{PPX}$ *3 | $V_{PPX}$ | Write (×8 No.2) | $D_{IN}$ (Upper Byte) | High-Z | NP |
| L | L | X | L | H | X | $V_{PPX}$ *3 | $V_{PPX}$ *3 | Read (×16) | $D_{OUT}$ | | P or NP |
| L | L | X | H | L | L | $V_{PPX}$ *3 | $V_{PPX}$ *3 | Write (×16) | $D_{IN}$ | | NP |
| X | X | X | H | H | L | $V_{PPX}$ *3 | $V_{PPX}$ *3 | Output Disable | High-Z | | P or NP |

**Notes:** *1. H = $V_{IH}$, L = $V_{IL}$, X = Either $V_{IL}$ or $V_{IH}$, WP SW = Write Protect Switch, P = Protect, NP = Non Protect
*2. L-level is output when WP SW = NP. H-level is output when WP SW = P.
*3. $V_{PP}$ must be $V_{PPH}$ at Program/Erase cycle.

**ATTRIBUTE MEMORY FUNCTION *1 ($\overline{REG}$ = $V_{IL}$) *2**

| $\overline{CE_2}$ | $\overline{CE_1}$ | $A_0$ | $\overline{OE}$ | $\overline{WE}$ | WP | Mode | Data Input/Output | | WP SW |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | $D_{15}$ to $D_8$ | $D_7$ to $D_0$ | |
| H | H | X | X | X | L | Standby | High-Z | | NP |
| H | L | L | L | H | L | Read (×8 No.1) | High-Z | $D_{OUT}$ *3 (Lower Byte) | NP |
| H | L | H | L | H | L | Read (×8 No.1) | High-Z | H | NP |
| H | L | L | H | L | L | Write (×8 No.1) | High-Z | $D_{IN}$ *4 (Lower Byte) | NP |
| H | L | H | H | L | L | Write (×8 No.1) | High-Z | X | NP |
| L | H | X | L | H | L | Read (×8 No.2) | H | High-Z | NP |
| L | H | X | H | L | L | Write (×8 No.2) | High-Z | High-Z | NP |
| L | L | X | L | H | L | Read (×16) | H | $D_{OUT}$ *3 (Lower Byte) | NP |
| L | L | X | H | L | L | Write (×16) | X | $D_{IN}$ *4 (Lower Byte) | NP |
| X | X | X | H | H | L | Output Disable | High-Z | | NP |
| H | H | X | X | X | H | Standby | High-Z | | P |
| H | L | L | L | H | H | Read (×8 No.1) | High-Z | $D_{OUT}$ *3 (Lower Byte) | P |
| H | L | H | L | H | H | Read (×8 No.1) | High-Z | H | P |
| H | L | L | H | L | H | Output Disable | High-Z | | P |
| H | L | H | H | L | H | Output Disable | High-Z | | P |
| L | H | X | L | H | H | Read (×8 No.2) | H | High-Z | P |
| L | H | X | H | L | H | Output Disable | High-Z | | P |
| L | L | X | L | H | H | Read (×16) | H | $D_{OUT}$ *3 (Lower Byte) | P |
| L | L | X | H | L | H | Output Disable | High-Z | | P |
| X | X | X | H | H | H | Output Disable | High-Z | | P |

**Notes:** *1. H = $V_{IH}$, L = $V_{IL}$, X = Either $V_{IL}$ or $V_{IH}$, WP SW = Write Protect Switch, P = Protect, NP = Non Protect

*2. N.C. for MB98A81131, 81231, 81331, and 81431.

*3. H-level is output for MB98A81132, 81232, 81332, and 81432.

*4. “X” for MB98A81132, 81232, 81332 and 81432.

# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ ADDRESS CONFIGURATIONS *1 (MAIN MEMORY)

### 8-BIT BUS ORGANIZATION No.1 ($\overline{CE_1}$ = $V_{IL}$, $\overline{CE_2}$ = $V_{IH}$)

| Chip Address $A_{23}$ to $A_{21}$, $A_0$ | Block Address $A_{20}$ to $A_{17}$ | Byte Address $A_{16}$ to $A_1$ | | | | $\overline{CE_2}$ | $\overline{CE_1}$ | $D_{15}$ to $D_8$ | $D_7$ to $D_0$ |
|---|---|---|---|---|---|---|---|---|---|
| 0000 | 0000 | 0000 | 0000 | 0000 | 0000 | H | L | – – – – – | 0 Add. |
| 0001 | 0000 | 0000 | 0000 | 0000 | 0000 | H | L | – – – – – | 1 Add. |
| 0000 | 0000 | 0000 | 0000 | 0000 | 0001 | H | L | – – – – – | 2 Add. |
| 0001 | 0000 | 0000 | 0000 | 0000 | 0001 | H | L | – – – – – | 3 Add. |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 1110 | 1111 | 1111 | 1111 | 1111 | 1110 | H | L | – – – – – | 16,777,212 Add. |
| 1111 | 1111 | 1111 | 1111 | 1111 | 1110 | H | L | – – – – – | 16,777,213 Add. |
| 1110 | 1111 | 1111 | 1111 | 1111 | 1111 | H | L | – – – – – | 16,777,214 Add. |
| 1111 | 1111 | 1111 | 1111 | 1111 | 1111 | H | L | – – – – – | 16,777,215 Add. |

### 8-BIT BUS ORGANIZATION No.2 ($\overline{CE_1}$ = $V_{IH}$, $\overline{CE_2}$ = $V_{IL}$) *2

| Chip Address $A_{23}$ to $A_{21}$, $A_0$ | Block Address $A_{20}$ to $A_{17}$ | Byte Address $A_{16}$ to $A_1$ | | | | $\overline{CE_2}$ | $\overline{CE_1}$ | $D_{15}$ to $D_8$ | $D_7$ to $D_0$ |
|---|---|---|---|---|---|---|---|---|---|
| 000X | 0000 | 0000 | 0000 | 0000 | 0000 | L | H | 1 Add. | – – – – – |
| 000X | 0000 | 0000 | 0000 | 0000 | 0001 | L | H | 3 Add. | – – – – – |
| 000X | 0000 | 0000 | 0000 | 0000 | 0010 | L | H | 5 Add. | – – – – – |
| 000X | 0000 | 0000 | 0000 | 0000 | 0011 | L | H | 7 Add. | – – – – – |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 111X | 1111 | 1111 | 1111 | 1111 | 1100 | L | H | 16,777,209 Add. | – – – – – |
| 111X | 1111 | 1111 | 1111 | 1111 | 1101 | L | H | 16,777,211 Add. | – – – – – |
| 111X | 1111 | 1111 | 1111 | 1111 | 1110 | L | H | 16,777,213 Add. | – – – – – |
| 111X | 1111 | 1111 | 1111 | 1111 | 1111 | L | H | 16,777,215 Add. | – – – – – |

### 16-BIT BUS ORGANIZATION ($\overline{CE_1}$ = $V_{IL}$, $\overline{CE_2}$ = $V_{IL}$)

| Chip Address $A_{23}$ to $A_{21}$, $A_0$ | Block Address $A_{20}$ to $A_{17}$ | Byte Address $A_{16}$ to $A_1$ | | | | $\overline{CE_2}$ | $\overline{CE_1}$ | $D_{15}$ to $D_8$ | $D_7$ to $D_0$ |
|---|---|---|---|---|---|---|---|---|---|
| 000X | 0000 | 0000 | 0000 | 0000 | 0000 | L | L | 1 Add. | 0 Add. |
| 000X | 0000 | 0000 | 0000 | 0000 | 0001 | L | L | 3 Add. | 2 Add. |
| 000X | 0000 | 0000 | 0000 | 0000 | 0010 | L | L | 5 Add. | 4 Add. |
| 000X | 0000 | 0000 | 0000 | 0000 | 0011 | L | L | 7 Add. | 6 Add. |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 111X | 1111 | 1111 | 1111 | 1111 | 1100 | L | L | 16,777,209 Add. | 16,777,208 Add. |
| 111X | 1111 | 1111 | 1111 | 1111 | 1101 | L | L | 16,777,211 Add. | 16,777,210 Add. |
| 111X | 1111 | 1111 | 1111 | 1111 | 1110 | L | L | 16,777,213 Add. | 16,777,212 Add. |
| 111X | 1111 | 1111 | 1111 | 1111 | 1111 | L | L | 16,777,215 Add. | 16,777,214 Add. |

**Notes:** *1. H = $V_{IH}$, L = $V_{IL}$, X = Either 0 or 1. $\overline{REG}$ = “H”.

*2. Even addresses can not be selected.

## ■ ADDRESS CONFIGURATIONS *1 (ATTRIBUTE MEMORY)

### 8-BIT BUS ORGANIZATION No.1 ($\overline{CE_1}$ = $V_{IL}$, $\overline{CE_2}$ = $V_{IH}$)

| $A_{23}$ to $A_{14}$ | $A_{13}$ to $A_0$ | $\overline{CE_2}$ | $\overline{CE_1}$ | $D_{15}$ to $D_8$ | $D_7$ to $D_0$ |
|---|---|---|---|---|---|
| XX —— XX | 0 —— 0000 | H | L | – – – – – | 0 Add. |
| XX —— XX | 0 —— 0001 | H | L | – – – – – | – – – – |
| XX —— XX | 0 —— 0010 | H | L | – – – – – | 2 Add. |
| XX —— XX | 0 —— 0011 | H | L | – – – – – | – – – – |
| ↓ ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| XX —— XX | 1 —— 1100 | H | L | – – – – – | 16,380 Add. |
| XX —— XX | 1 —— 1101 | H | L | – – – – – | – – – – |
| XX —— XX | 1 —— 1110 | H | L | – – – – – | 16,382 Add. |
| XX —— XX | 1 —— 1111 | H | L | – – – – – | – – – – |

### 8-BIT BUS ORGANIZATION No.2 ($\overline{CE_1}$ = $V_{IH}$, $\overline{CE_2}$ = $V_{IL}$) *2

| $A_{23}$ to $A_{14}$ | $A_{13}$ to $A_0$ | $\overline{CE_2}$ | $\overline{CE_1}$ | $D_{15}$ to $D_8$ | $D_7$ to $D_0$ |
|---|---|---|---|---|---|
| XX —— XX | 0 —— 000X | L | H | – – – – – | – – – – – |
| XX —— XX | 0 —— 001X | L | H | – – – – – | – – – – – |
| XX —— XX | 0 —— 010X | L | H | – – – – – | – – – – – |
| XX —— XX | 0 —— 011X | L | H | – – – – – | – – – – – |
| ↓ ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| XX —— XX | 1 —— 100X | L | H | – – – – – | – – – – – |
| XX —— XX | 1 —— 101X | L | H | – – – – – | – – – – – |
| XX —— XX | 1 —— 110X | L | H | – – – – – | – – – – – |
| XX —— XX | 1 —— 111X | L | H | – – – – – | – – – – – |

### 16-BIT BUS ORGANIZATION ($\overline{CE_1}$ = $V_{IL}$, $\overline{CE_2}$ = $V_{IL}$)

| $A_{23}$ to $A_{14}$ | $A_{13}$ to $A_0$ | $\overline{CE_2}$ | $\overline{CE_1}$ | $D_{15}$ to $D_8$ | $D_7$ to $D_0$ |
|---|---|---|---|---|---|
| XX —— XX | 0 —— 000X | L | L | – – – – – | 0 Add. |
| XX —— XX | 0 —— 001X | L | L | – – – – – | 2 Add. |
| XX —— XX | 0 —— 010X | L | L | – – – – – | 4 Add. |
| XX —— XX | 0 —— 011X | L | L | – – – – – | 6 Add. |
| ↓ ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| XX —— XX | 1 —— 100X | L | L | – – – – – | 16,376 Add. |
| XX —— XX | 1 —— 101X | L | L | – – – – – | 16,378 Add. |
| XX —— XX | 1 —— 110X | L | L | – – – – – | 16,380 Add. |
| XX —— XX | 1 —— 111X | L | L | – – – – – | 16,382 Add. |

**Notes:** *1. H = $V_{IH}$, L = $V_{IL}$, X = Either 0 or 1.

*2. Attribute memory can not be accessed.

# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ PROGRAM/ERASE CHIP DECODING TABLE

| Bus Organization | $\overline{CE}_2$ | $\overline{CE}_1$ | $A_{23}$ | $A_{22}$ | $A_{21}$ | $A_0$ | Decode Chips |
|---|---|---|---|---|---|---|---|
| 8-bit Bus | H | L | L | L | L | L | Chip 0 |
| | | | | | | H | Chip 1 |
| | | | | | H | L | Chip 2 |
| | | | | | | H | Chip 3 |
| | | | | H | L | L | Chip 4 |
| | | | | | | H | Chip 5 |
| | | | | | H | L | Chip 6 |
| | | | | | | H | Chip 7 |
| | | | H | L | L | L | Chip 8 |
| | | | | | | H | Chip 9 |
| | | | | | H | L | Chip 10 |
| | | | | | | H | Chip 11 |
| | | | | H | L | L | Chip 12 |
| | | | | | | H | Chip 13 |
| | | | | | H | L | Chip 14 |
| | | | | | | H | Chip 15 |
| | L | H | L | L | L | X | Chip 1 |
| | | | | | H | | Chip 3 |
| | | | | H | L | | Chip 5 |
| | | | | | H | | Chip 7 |
| | | | H | L | L | | Chip 9 |
| | | | | | H | | Chip 11 |
| | | | | H | L | | Chip 13 |
| | | | | | H | | Chip 15 |
| 16-bit Bus | L | L | L | L | L | X | Chip 0, Chip 1 |
| | | | | | H | | Chip 2, Chip 3 |
| | | | | H | L | | Chip 4, Chip 5 |
| | | | | | H | | Chip 6, Chip 7 |
| | | | H | L | L | | Chip 8, Chip 9 |
| | | | | | H | | Chip 10, Chip 11 |
| | | | | H | L | | Chip 12, Chip 13 |
| | | | | | H | | Chip 14, Chip 15 |

**Note:** H = $V_{IH}$, L = $V_{IL}$, X = Either $V_{IH}$ or $V_{IL}$

## ■ ERASE BLOCK DECODING TABLE

| $A_{20}$ | $A_{19}$ | $A_{18}$ | $A_{17}$ | Decode Block |
|---|---|---|---|---|
| L | L | L | L | Block 0 |
| | | | H | Block 1 |
| | | H | L | Block 2 |
| | | | H | Block 3 |
| | H | L | L | Block 4 |
| | | | H | Block 5 |
| | | H | L | Block 6 |
| | | | H | Block 7 |
| H | L | L | L | Block 8 |
| | | | H | Block 9 |
| | | H | L | Block 10 |
| | | | H | Block 11 |
| | H | L | L | Block 12 |
| | | | H | Block 13 |
| | | H | L | Block 14 |
| | | | H | Block 15 |

**Note:** H = $V_{IH}$, L = $V_{IL}$, X = Either $V_{IH}$ or $V_{IL}$

## ■ CARD CHIP/BLOCK CONFIGURATION

| $D_{15}$ ◄—— $D_8$ | $D_7$ ◄—— $D_0$ | |
|---|---|---|
| UPPER BYTE | LOWER BYTE | ×16 bit mode |
| ODD BYTE | EVEN BYTE | ×8 bit mode |

| | |
|---|---|
| Chip 15 | Chip 14 |
| Chip 13 | Chip 12 |
| Chip 11 | Chip 10 |
| Chip 9 | Chip 8 |
| Chip 7 | Chip 6 |
| Chip 5 | Chip 4 |
| Chip 3 | Chip 2 |
| **Chip 1** | **Chip 0** |

**Card Chip Configuration for 16 MB Card**

| **Chip 1** (8 M Flash Chip) | **Chip 0** (8 M Flash Chip) |
|---|---|
| Block 15 (64 K × 8 bits) | Block 15 (64 K × 8 bits) |
| Block 14 (64 K × 8 bits) | Block 14 (64 K × 8 bits) |
| Block 13 (64 K × 8 bits) | Block 13 (64 K × 8 bits) |
| • • • • • • | • • • • • • |
| Block 2 (64 K × 8 bits) | Block 2 (64 K × 8 bits) |
| Block 1 (64 K × 8 bits) | Block 1 (64 K × 8 bits) |
| Block 0 (64 K × 8 bits) | Block 0 (64 K × 8 bits) |

**Block Configuration for 2 Chips**

## ■ COMMAND DEFINITION TABLE

### Command Table for 8-bit Mode

| Command | Bus Cycle Required | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|
| | | Operation *1 | Address *2 | Data *3 | Operation *1 | Address *2 | Data *3 |
| Read Memory/Reset | 1 | Write | DA | FFH | — | — | — |
| Read Intelligent ID Codes *4 | 3 | Write | DA | 90H | Read | IA | ID |
| Setup Erase/Erase *5 | 2 | Write | ZA | 20H | Write | ZA | D0H |
| Erase Suspend *7 /Erase Resume | 2 | Write | DA | B0H | Write | DA | D0H |
| Setup Program/ Program *6 | 2 | Write | WA | 40H | Write | WA | WD |
| Alternate Setup Program/Program *6 | 2 | Write | WA | 10H | Write | WA | WD |
| Read Status Register | 2 | Write | DA | 70H | Read | DA | SRD |
| Clear Status Register | 1 | Write | DA | 50H | — | — | — |

### Command Table for 16-bit Mode

| Command | Bus Cycle Required | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|
| | | Operation *1 | Address *2 | Data *3 | Operation *1 | Address *2 | Data *3 |
| Read Memory/Reset | 1 | Write | DA | FFFFH | — | — | — |
| Read Intelligent ID Codes *4 | 3 | Write | DA | 9090H | Read | IA | ID |
| Setup Erase/Erase *5 | 2 | Write | ZA | 2020H | Write | ZA | D0D0H |
| Erase Suspend *7 /Erase Resume | 2 | Write | DA | B0B0H | Write | DA | D0D0H |
| Setup Program/ Program *6 | 2 | Write | WA | 4040H | Write | WA | WD |
| Alternate Setup Program/Program *6 | 2 | Write | WA | 1010H | Write | WA | WD |
| Read Status Register | 2 | Write | DA | 7070H | Read | DA | SRD |
| Clear Status Register | 1 | Write | DA | 5050H | — | — | — |

**Notes:** *1. Bus operations are defined in “FUNCTIONAL TRUTH TABLE”.

*2. DA = Address in selected chip
IA = Identifier address: 00H for manufacturer code, 01H for device code.
WA = Address of memory location to be programmed.
ZA = Address of 128 K-Byte zones involved in erase operation.
Addresses are latched on the rising edge of the Write Enable pulse or Card Enable pulse.

*3. ID = Data read from location IA during device identification.
Manufacturer = 89H for 8-bit, 8989H for 16-bit/Device = A2H for 8-bit, A2A2H for 16-bit
SRD = Data of Status Register.
WD = Data to be programmed at location WA. Data is latched on the rising edge of Write Enable or Card Enable.

*4. Following the Read Intelligent ID command, two read operations access manufacturer and device codes.

*5. “ERASE FLOWCHART” in Fig.5 illustrates the Erase Algorithm.

*6. “PROGRAM FLOWCHART” in Fig.4 illustrates the Program Algorithm.

*7. “ERASE SUSPEND LOOP” in Fig.6 illustrates the Erase Suspend Algorithm.

## ■ STATUS REGISTER DEFINITIONS

### 8-BIT BUS ORGANIZATION

| STATUS REGISTER | WSMS | ESS | ES | BPS | VPPS | R | R | R |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

### 16-BIT BUS ORGANIZATION

| STATUS REGISTER | WSMS | ESS | ES | BPS | VPPS | R | R | R |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **STATUS REGISTER** | **WSMS** | **ESS** | **ES** | **BPS** | **VPPS** | **R** | **R** | **R** |
| BIT | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |

WSMS (Write State Machine Status) 1 = Ready 0 = Busy
Byte write or block erase completion can be checked with WSMS bit.
“1” of Ready status is output at erase suspended condition.

ESS (Erase Suspend Status) 1 = Erase Suspended 0 = Erase In Process/Completed
When Erase operation is suspended, “1” is output from ESS bit.

ES (Erase Status) 1 = Error in Block Erase 0 = Successful Block Erase
ES bit indicates whether the erase operation was successfully performed.

BPS (Byte Program Status) 1 = Error in Byte Program 0 = Successful Byte Program
BPS bit indicates whether the byte program operation was successfully performed.

VPPS (VPPS Status) 1 = $V_{PP}$ Low Detect; Operation Abort 0 = $V_{PP}$ OK
VPPS bit indicates $V_{PP}$ status before program/erase operation, and does not detect the status in program/erase operation.

R (Reserve)
“0” is output during Status Register output.

### Clear Status Register Command

ES, BPS and VPPS are cleared by input of Clear Status Register Command. These Status Register bits must be cleared before Program/Erase operations are executed.

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Note | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | –0.5 to +6.0 | V |
| Input Voltage | | $V_{IN}$ | –0.5 to $V_{CC}$ +0.5 | V |
| Output Voltage | | $V_{OUT}$ | –0.5 to $V_{CC}$ +0.5 | V |
| Programming Voltage | *1 | $V_{PP1}$, $V_{PP2}$ | –2.0 to +14.0 | V |
| Ambient Temperature | | $T_A$ | 0 to +60 | °C |
| Storage Temperature | | $T_{STG}$ | –30 to +70 | °C |

**Note:** *1. Minimum DC input voltage is –0.5 V.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Notes | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ Supply Voltage | | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V |
| Ground | | GND | — | 0 | — | V |
| Input Low Voltage | | $V_{IL}$ | –0.3 | — | 0.8 | V |
| Input High Voltage | | $V_{IH}$ | 2.4 | — | $V_{CC}$ +0.3 | V |
| $V_{PP}$ during Read-Only Operation | *1 | $V_{PPL}$ | 0 | — | 6.5 | V |
| $V_{PP}$ during Program/Erase Operation | | $V_{PPH}$ | 11.4 | 12.0 | 12.6 | V |
| Ambient Temperature | | $T_A$ | 0 | — | 55 | °C |

**Note:** *1. Program/Erase are inhibited when $V_{PP} = V_{PPL}$.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ CAPACITANCE

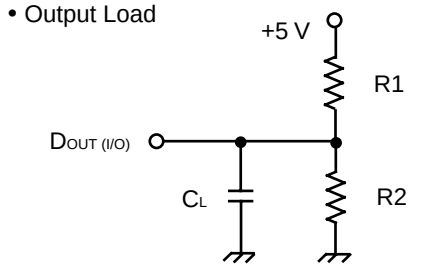
($T_A$ = 25°C, f = 1 MHz, $V_{IN} = V_{I/O}$ = GND)

| Parameter | Notes | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Input Capacitance | *1 | $C_{IN}$ | — | 50 | pF |
| I/O Capacitance | *2 | $C_{I/O}$ | — | 50 | pF |

**Notes:** *1. This value does not apply to $\overline{CE}_1$, $\overline{CE}_2$, $\overline{WE}$ and $\overline{REG}$.

*2. This value does not apply to $\overline{CE}_1$, $\overline{CE}_2$, BVD1 and BVD2.

**Fig. 3 – AC TEST CONDITIONS**




- Input Pulse Levels: $V_{IH}$ = 2.6 V, $V_{IL}$ = 0.6 V
- Input Pulse Rise and Fall Times: 5 ns (Transient between 0.8 V and 2.4 V)
- Timing Reference Levels

  Input: $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.4 V
  Output: $V_{OL}$ = 0.8 V, $V_{OH}$ = 2.0 V

* Including jig and stray capacitance

| | R1 | R2 | $C_L$ | Parameter Measured |
|---|---|---|---|---|
| Load I | 1.8 kΩ | 990 Ω | 100 pF | All parameters except $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{RCLZ}$, $t_{ROLZ}$, $t_{RCHZ}$ and $t_{ROHZ}$ |
| Load II | 1.8 kΩ | 990 Ω | 5 pF | $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{RCLZ}$, $t_{ROLZ}$, $t_{RCHZ}$ and $t_{ROHZ}$ |

# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ DC CHARACTERISTICS

| Parameter | Notes | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Input Leakage Current | *1 | $I_{LI}$ | $V_{CC} = V_{CC}$ max<br>$V_{IN}$ = 0 V or $V_{CC}$ | — | ±1.0 | ±20 | µA |
| Output Leakage Current | *2 | $I_{LO}$ | $V_{CC} = V_{CC}$ max<br>$V_{IN}$ = 0 V or $V_{CC}$ | — | ±1.0 | ±20 | µA |
| Standby Current | | $I_{SB1}$ | $V_{CC} = V_{CC}$ max<br>$\overline{CE}_1 = \overline{CE}_2 = V_{CC} - 0.2$ V | — | 0.5 | 1.7 | mA |
| | | $I_{SB2}$ | $V_{CC} = V_{CC}$ max<br>$\overline{CE}_1 = \overline{CE}_2 = V_{IH}$ | — | 4.0 | 8.0 | mA |
| Active Read Current | | $I_{CC1}$ | $V_{CC} = V_{CC}$ max<br>$\overline{CE}_1 = \overline{CE}_2 = V_{IL}$<br>Cycle = 200 ns<br>$I_{OUT}$ = 0 mA | — | 110 | 150 | mA |
| Program Current | | $I_{CC2}$ | Program in progress | — | 20 | 60 | mA |
| Erase Current | | $I_{CC3}$ | Erase in progress | — | 20 | 60 | mA |
| Erase Suspend Current | *4 | $I_{CCES}$ | Erase Suspend<br>$\overline{CE}_1 = \overline{CE}_2 = V_{IH}$ | — | 10 | 20 | mA |
| $V_{PP}$ Read Current or Standby Current | *5 | $I_{PP1}$ | $V_{PP} > V_{CC}$ | — | 0.9 | 1.8 | mA |
| | | | $V_{PP} \leq V_{CC}$ | — | — | 175 | µA |
| $V_{PP}$ Program Current | *5 | $I_{PP2}$ | $V_{PP} = V_{PPH}$<br>Program in progress | — | 10 | 30 | mA |
| $V_{PP}$ Erase Current | *5 | $I_{PP3}$ | $V_{PP} = V_{PPH}$<br>Erase in progress | — | 10 | 30 | mA |
| Output Low Voltage | | $V_{OL}$ | $I_{OL}$ = 3.2 mA<br>$V_{CC} = V_{CC}$ min | — | — | 0.4 | V |
| Output High Voltage | *3 | $V_{OH}$ | $I_{OH}$ = –2.0 mA<br>$V_{CC} = V_{CC}$ min | 3.8 | — | — | V |

**Notes:** *1. This value does not apply to $\overline{CE}_1$, $\overline{CE}_2$, $\overline{WE}$ and $\overline{REG}$.
*2. This value does not apply to BVD1, BVD2, $\overline{CD}_1$ and $\overline{CD}_2$.
*3. This value does not apply to BVD1 and BVD2.
*4. The read current during erase-suspend operation = $I_{CCES}$ + $I_{CC1}$.
*5. These values for $V_{PP1}$ and $V_{PP2}$.

## ■ AC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.)**

### MAIN MEMORY PROGRAM/ERASE PERFORMANCE

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Block Erase Time | — | 1.6 * | 10 | Sec. |
| Block Program Time | — | 0.6 * | 2.1 | Sec. |
| Program/Erase Cycle | 10,000 | 100,000 | — | Cycle |

* : The conditions of typical values are $T_A$ = 25°C, $V_{PP}$ = 12 V, 10,000 cycles by algorithm).

### ATTRIBUTE MEMORY PROGRAM PERFORMANCE

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Byte Program Time | — | — | 10 | mS |
| Number of Program per Byte | 10,000 | — | — | Times |

### MAIN MEMORY READ CYCLE *1

| Parameter | Notes | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Read Cycle Time | | $t_{RC}$ | 200 | — | ns |
| Card Enable Access Time | | $t_{CE}$ | — | 200 | ns |
| Address Access Time | | $t_{ACC}$ | — | 200 | ns |
| Output Enable Access Time | | $t_{OE}$ | — | 100 | ns |
| Card Enable to Output in Low-Z | *2 | $t_{CLZ}$ | 5 | — | ns |
| Card Disable to Output in High-Z | *2 | $t_{CHZ}$ | — | 60 | ns |
| Output Enable to Output in Low-Z | *2 | $t_{OLZ}$ | 5 | — | ns |
| Output Disable to Output in High-Z | *2 | $t_{OHZ}$ | — | 60 | ns |
| Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change | *3 | $t_{OH}$ | 5 | — | ns |

### ATTRIBUTE MEMORY READ CYCLE *1*4

| Parameter | Notes | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Read Cycle Time | | $t_{RRC}$ | 300 | — | ns |
| Address Access Time | | $t_{RAA}$ | — | 300 | ns |
| Card Enable Access Time | | $t_{RCE}$ | — | 300 | ns |
| Output Enable Access Time | | $t_{ROE}$ | — | 150 | ns |
| Output Hold from Address Change | | $t_{ROH}$ | 5 | — | ns |
| Card Enable to Output Low-Z | *2 | $t_{RCLZ}$ | 5 | — | ns |
| Output Enable to Output Low-Z | *2 | $t_{ROLZ}$ | 5 | — | ns |
| Card Enable to Output High-Z | *2 | $t_{RCHZ}$ | — | 60 | ns |
| Output Enable to Output High-Z | *3 | $t_{ROHZ}$ | — | 60 | ns |

**Notes:** *1. Rise/Fall time < 5 ns.

*2. Transition is measured at the point of ±500 mV from steady state voltage. This parameter is specified using Load II in Fig.3.

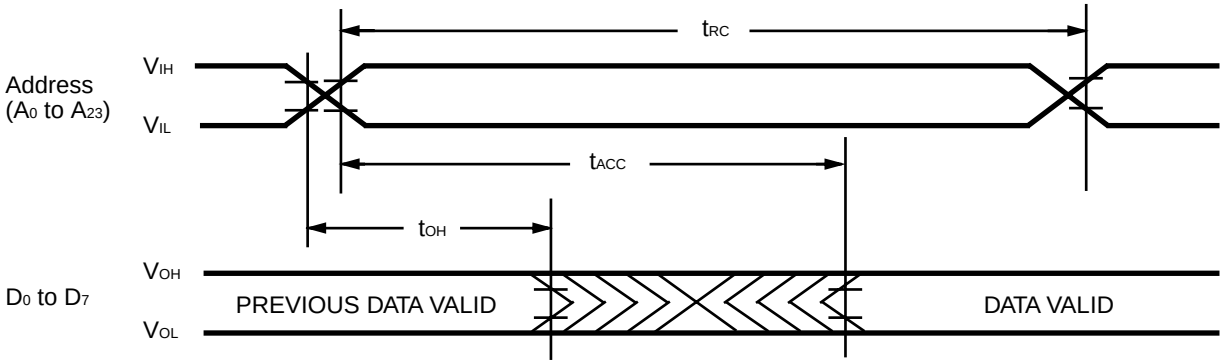
*3. This parameter is specified from the rising edge of $\overline{OE}$, $\overline{CE_1}$ and $\overline{CE_2}$, whichever occurs first.

*4. This parameter is for MB98A81133, 81233, 81333, and 81433.

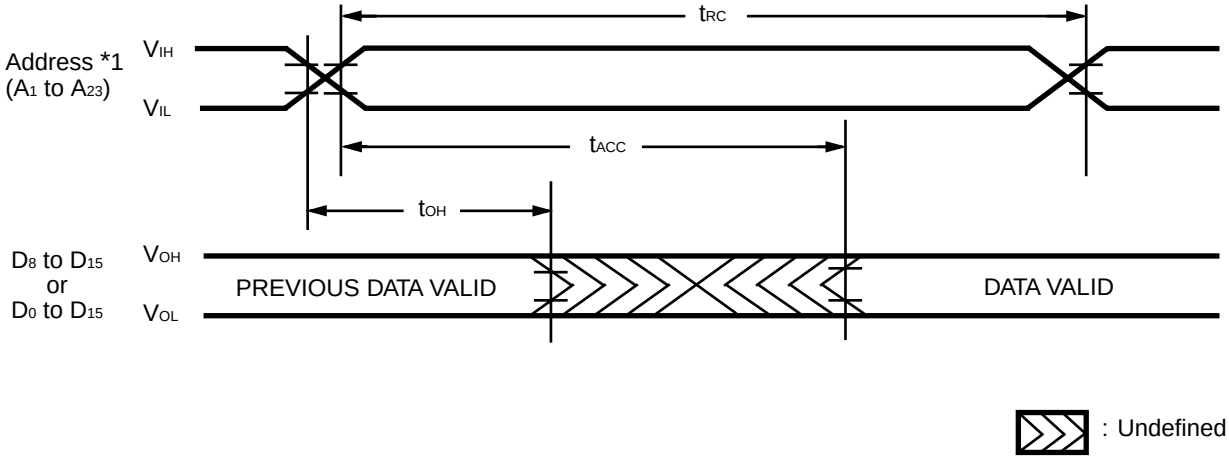
# MB98A8113x-/8123x-/8133x-/8143x-20

## MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = $V_{IH}$, $\overline{REG}$ = $V_{IH}$)

READ CYCLE 1: $\overline{CE_1}$ = $\overline{OE}$ = $V_{IL}$, $\overline{CE_2}$ = $V_{IH}$: × 8-bit No.1 Bus Organization



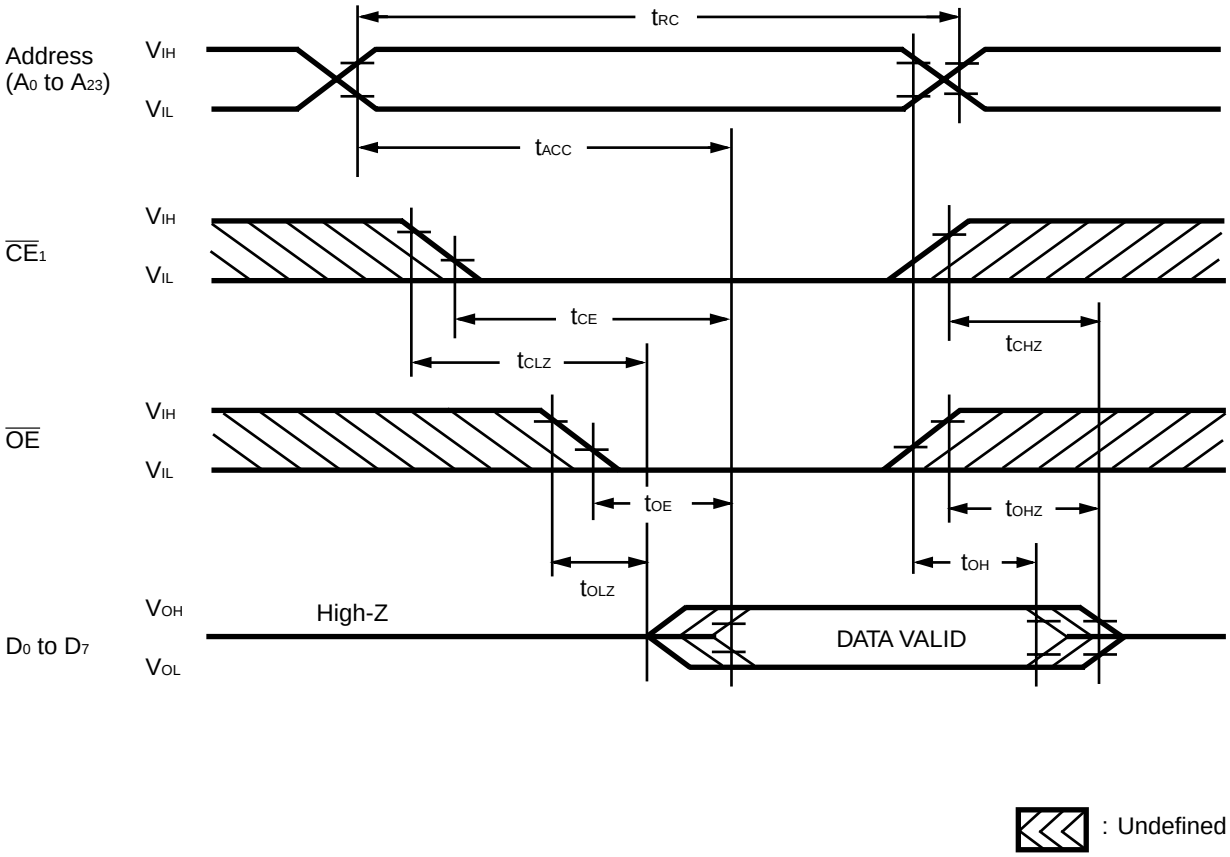

READ CYCLE 2: $\overline{CE_1}$ = $V_{IH}$, $\overline{CE_2}$ = $\overline{OE}$ = $V_{IL}$: × 8-bit No.2 Bus Organization
$\overline{CE_1}$ = $\overline{CE_2}$ = $\overline{OE}$ = $V_{IL}$: × 16-bit Bus Organization




**Note:** *1. $A_0$ = Either $V_{IH}$ or $V_{IL}$.

## MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = $V_{IH}$, $\overline{REG}$ = $V_{IH}$)

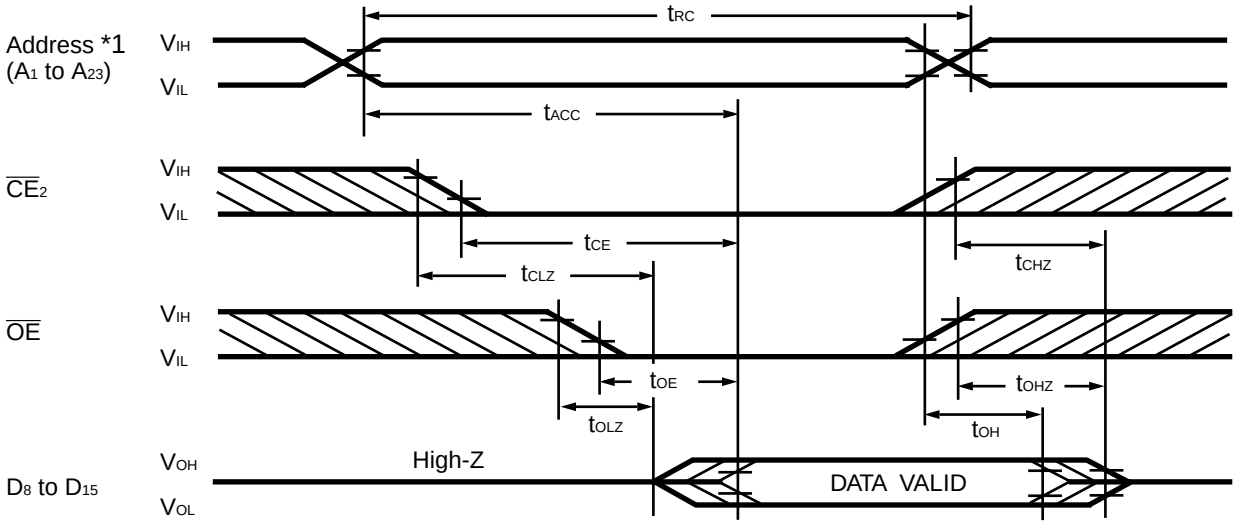
READ CYCLE 3: $\overline{CE_2}$ = $V_{IH}$: × 8-bit No.1 Bus Organization



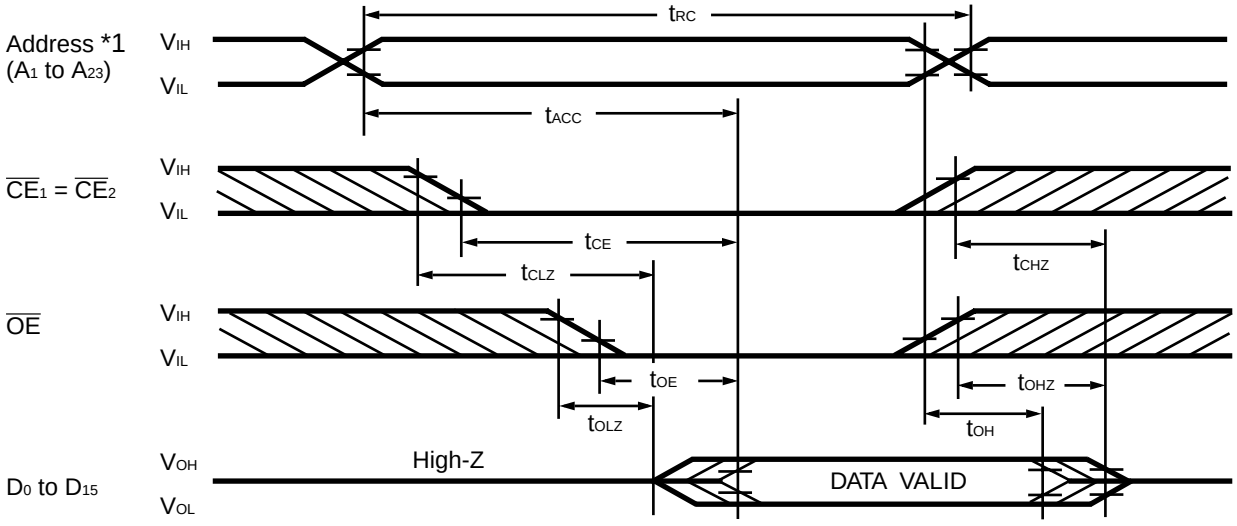
# MB98A8113x-/8123x-/8133x-/8143x-20

## MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = $V_{IH}$, $\overline{REG}$ = $V_{IH}$)

READ CYCLE 4: $\overline{CE_1}$ = $V_{IH}$: × 8-bit No.2 Bus Organization




READ CYCLE 5: $\overline{CE_1}$ = $\overline{CE_2}$ = $V_{IL}$: × 16-bit Bus Organization

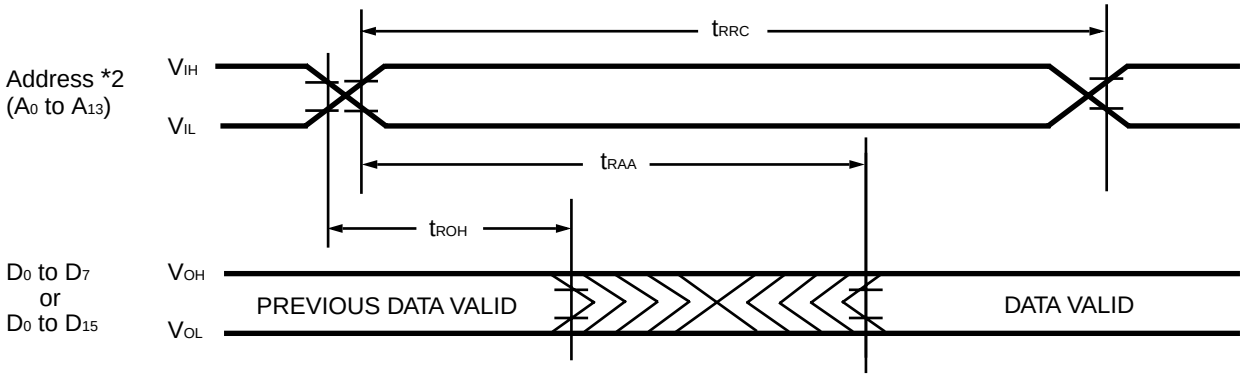



: Undefined

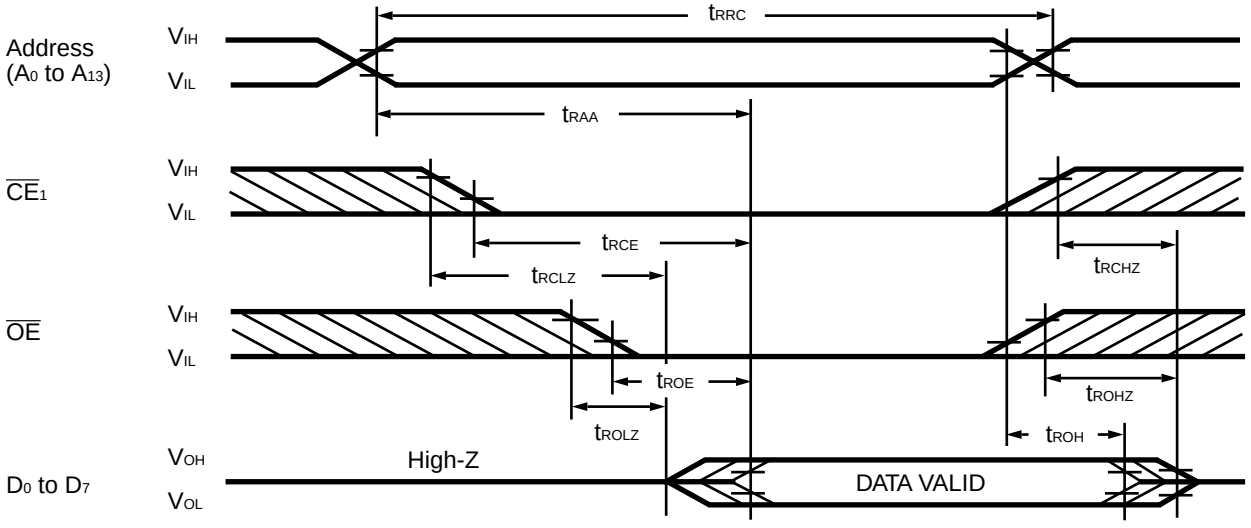
**Note:** *1. $A_0$ = Either $V_{IL}$ or $V_{IH}$.

## ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = $V_{IH}$, $\overline{REG}$ = $V_{IL}$) *1

READ CYCLE 1: $\overline{CE_1}$ = $\overline{OE}$ = $V_{IL}$, $\overline{CE_2}$ = $V_{IH}$: × 8-bit No.1 Bus Organization
$\overline{CE_1}$ = $\overline{CE_2}$ = $\overline{OE}$ = $V_{IL}$: × 16-bit Bus Organization




READ CYCLE 2: $\overline{CE_2}$ = $V_{IH}$: × 8-bit No.1 Bus Organization



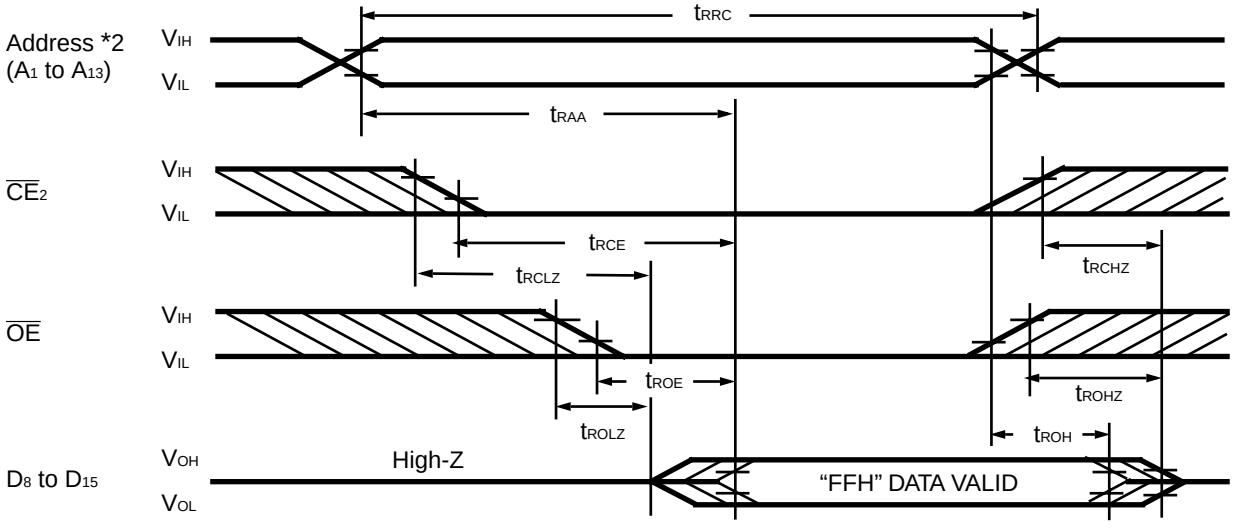

**Notes:** *1. This timing diagram is for MB98A81133, 81233, 81333, and 81433. “FF” data is available on MB98A81132, 81232, 81332, and 81432 only.

*2. $A_0$ = $V_{IL}$ or $V_{IH}$ at ×16-bit bus organization.

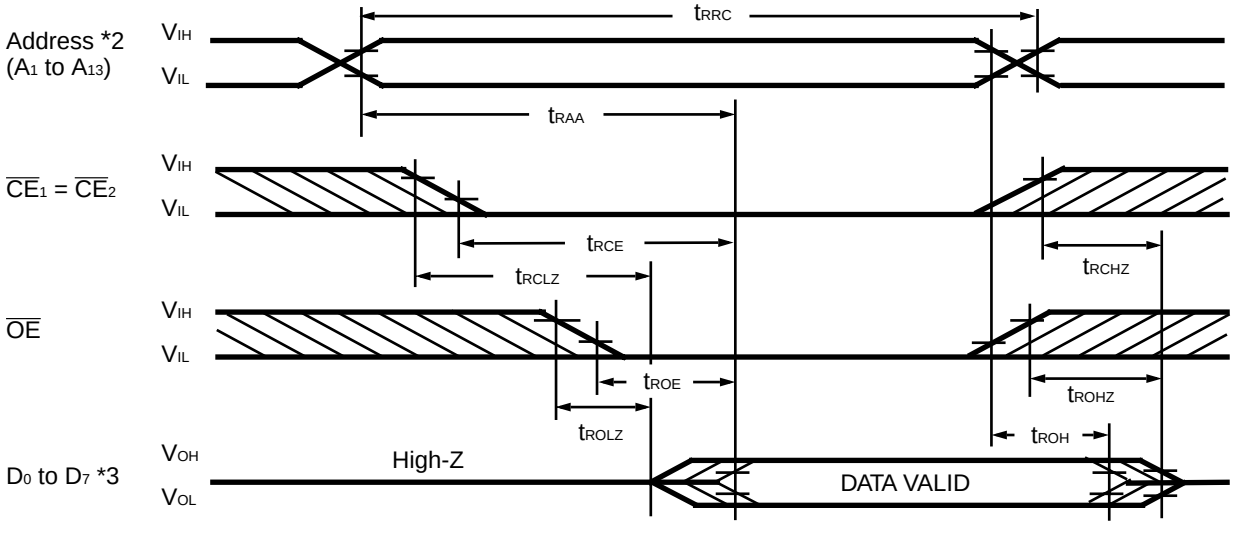
# MB98A8113x-/8123x-/8133x-/8143x-20

## ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = $V_{IH}$, $\overline{REG}$ = $V_{IL}$) *1

READ CYCLE 3: $\overline{CE_1}$ = $V_{IH}$: × 8-bit No.2 Bus Organization




READ CYCLE 4: $\overline{CE_1}$ = $\overline{CE_2}$: × 16-bit Bus Organization




: Undefined

**Notes:** *1. This timing diagram is for MB98A81133, 81233, 81333, and 81433. "FF" data is available on MB98A81132, 81232, 81332, and 81432 only.

*2. $A_0$ = Either $V_{IH}$ or $V_{IL}$.

*3. H-level is output from $D_8$ to $D_{15}$.

## MAIN MEMORY PROGRAM/ERASE CYCLE *1 *2

| Parameter | Notes | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Write Cycle Time | | $t_{WC}$ | 200 | — | ns |
| Address Set Up Time | | $t_{AS}$ | 100 | — | ns |
| Address Hold Time | | $t_{AH}$ | 30 | — | ns |
| Data Setup Time | | $t_{DS}$ | 80 | — | ns |
| Data Hold Time | | $t_{DH}$ | 25 | — | ns |
| Write Recovery Time before Read ($\overline{WE}$ control) | | $t_{WHGL}$ | 10 | — | µs |
| Write Recovery Time before Read ($\overline{CE}$ control) | | $t_{EHGL}$ | 10 | — | µs |
| Read Recover Time | | $t_{GHWL}$ | 0 | — | ns |
| Card Enable Setup Time before Write | | $t_{CS}$ | 0 | — | ns |
| Card Enable Hold Time | | $t_{CH}$ | 0 | — | ns |
| Write Enable Pulse Width | | $t_{WP}$ | 100 | — | ns |
| Write Enable Pulse Width High | | $t_{WPH}$ | 60 | — | ns |
| Write Enable Setup Time | | $t_{WS}$ | 0 | — | ns |
| Write Enable Hold Time | | $t_{WH}$ | 0 | — | ns |
| Card Enable Pulse Width | | $t_{CP}$ | 100 | — | ns |
| Card Enable Pulse Width High | | $t_{CPH}$ | 60 | — | ns |
| Duration of Byte Program Operation ($\overline{WE}$ Control) | *3 | $t_{WHQV1}$ | 6 | — | µs |
| Duration of Block Erase Operation ($\overline{WE}$ Control) | *3 | $t_{WHQV2}$ | 0.3 | — | s |
| Duration of Byte Program Operation ($\overline{CE}$ Control) | *3 | $t_{EHQV1}$ | 6 | — | µs |
| Duration of Block Erase Operation ($\overline{CE}$ Control) | *3 | $t_{EHQV2}$ | 0.3 | — | s |
| $V_{PP}$ Setup Time to Write Enable Low | | $t_{VPWH}$ | 100 | — | ns |
| $V_{PP}$ Setup Time to Chip Enable Low | | $t_{VPEH}$ | 100 | — | ns |
| $V_{PP}$ Hold Time | | $t_{QVVL}$ | 0 | — | ns |

**Notes:** *1. Read timing parameters during Program/Erase operations are the same as those during read only operations.
Refer to AC characteristics for Main Memory Read Cycle.

*2. Rise/Fall time ≤ 5 ns.

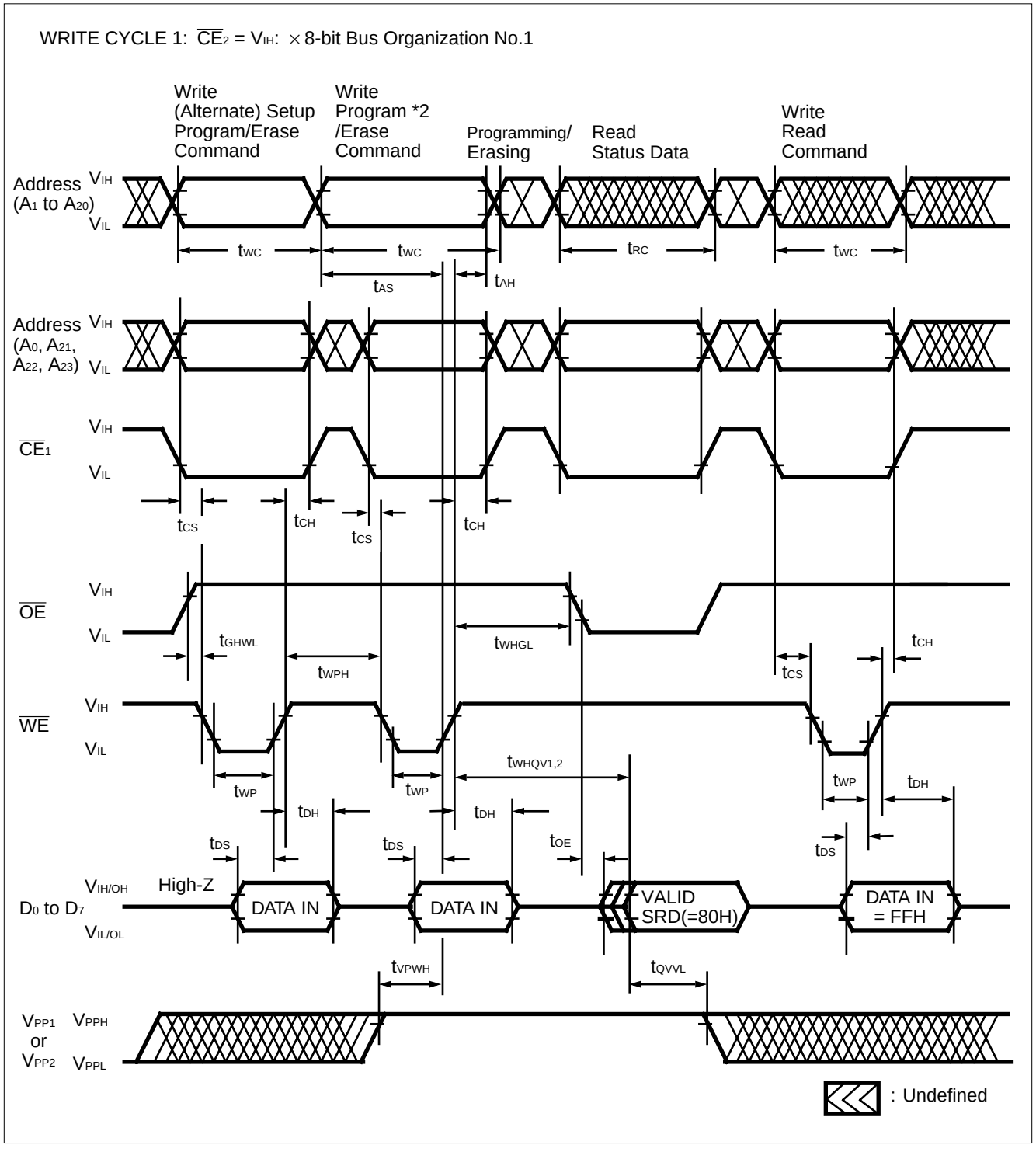
*3. The integrated stop timer terminates the Program/Erase operations, thereby eliminating the necessary for a maximum specification.

### ATTRIBUTE MEMORY PROGRAM CYCLE *1

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Address Setup Time | $t_{RAS}$ | 20 | — | ns |
| Card Enable Setup Time | $t_{RCS}$ | 0 | — | ns |
| Output Enable Setup Time | $t_{ROES}$ | 20 | — | ns |
| Write Pulse Width | $t_{RWP}$ | 100 | — | ns |
| Address Hold Time | $t_{RAH}$ | 50 | — | ns |
| Data Setup Time | $t_{RDS}$ | 50 | — | µs |
| Data Hold Time | $t_{RDH}$ | 20 | — | ns |
| Card Enable Hold Time | $t_{RCH}$ | 0 | — | ns |
| Output Enable Hold Time | $t_{ROEH}$ | 20 | — | ns |
| Program Time | $t_{RWR}$ | — | 10 | ms |
| Program Recovery Time | $t_{RRE}$ | 50 | — | ns |
| End of Program to Output Time | $t_{RRBO}$ | — | 100 | ns |
| Write Enable Hold Time | $t_{RWEH}$ | 10 | — | ns |

**Note:** *1. This parameter is for MB98A81133, 81233, 81333, and 81433.

## MAIN MEMORY PROGRAM & ERASE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = $V_{IH}$) *1

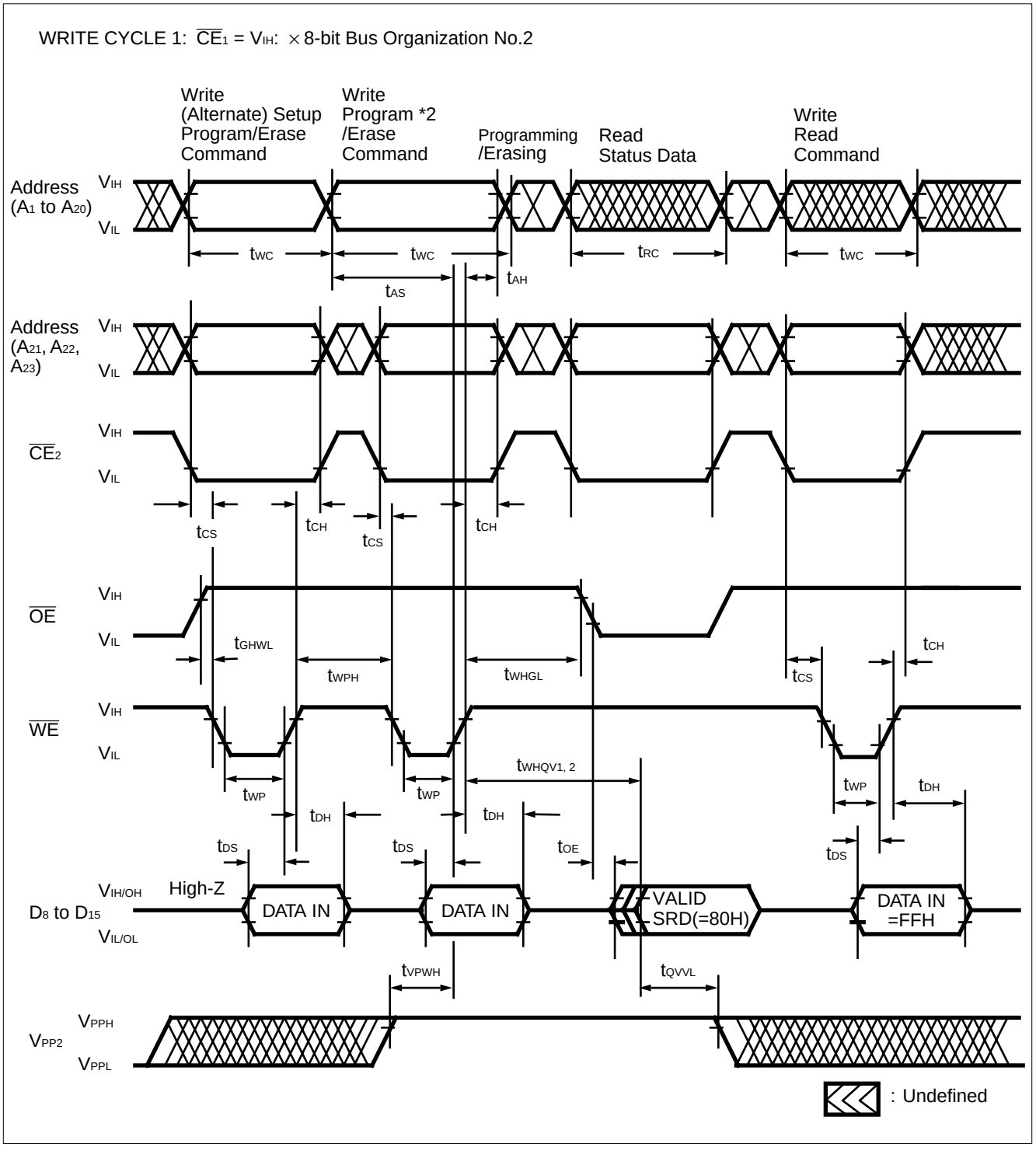



**Notes:** *1. $A_0$, $A_{21}$, $A_{22}$ and $A_{23}$ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the PROGRAM/ERASE CHIP DECODING INFORMATION.

*2. Latch address and data.

# MB98A8113x-/8123x-/8133x-/8143x-20

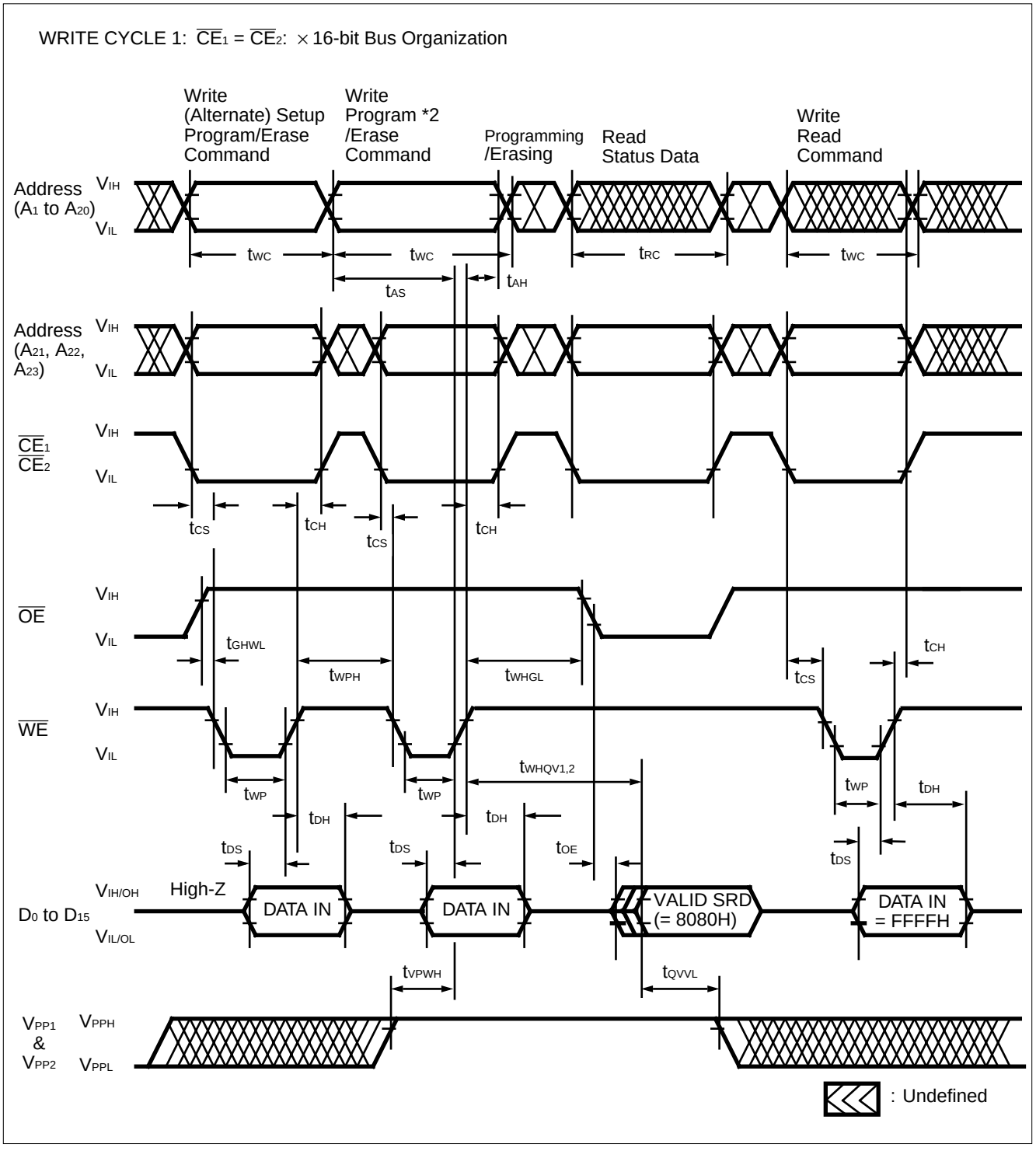
## MAIN MEMORY PROGRAM & ERASE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = $V_{IH}$) *1




**Notes:** *1. $A_{21}$, $A_{22}$ and $A_{23}$ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the PROGRAM/ERASE CHIP DECODING INFORMATION. $A_0$ = Either $V_{IL}$ or $V_{IH}$.

*2. Latch address and data.

## MAIN MEMORY PROGRAM & ERASE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = $V_{IH}$) *1

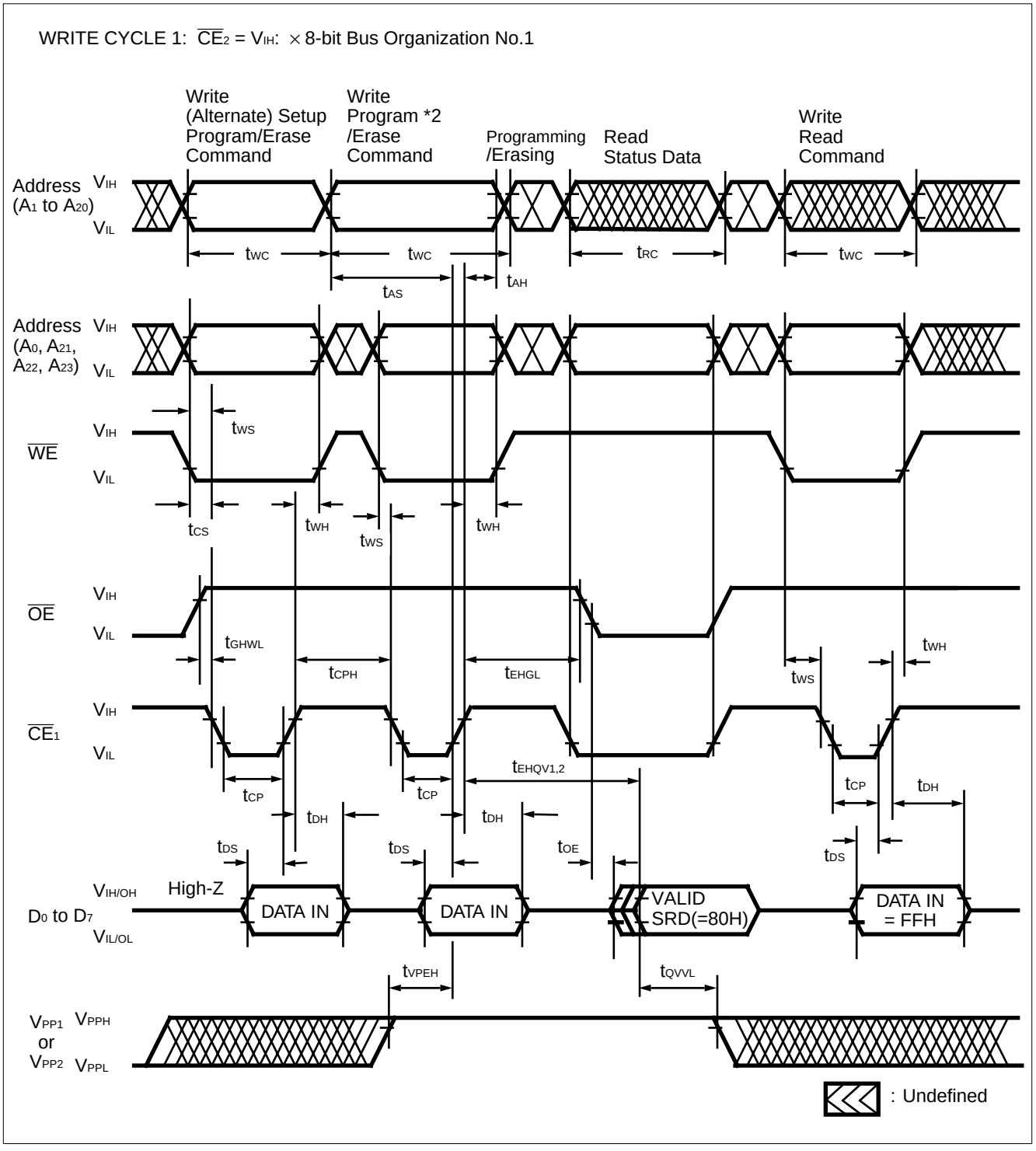



**Notes:** *1. $A_{21}$, $A_{22}$ and $A_{23}$ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the PROGRAM/ERASE CHIP DECODING INFORMATION. $A_0$ = Either $V_{IL}$ or $V_{IH}$.

*2. Latch address and data.

# MB98A8113x-/8123x-/8133x-/8143x-20

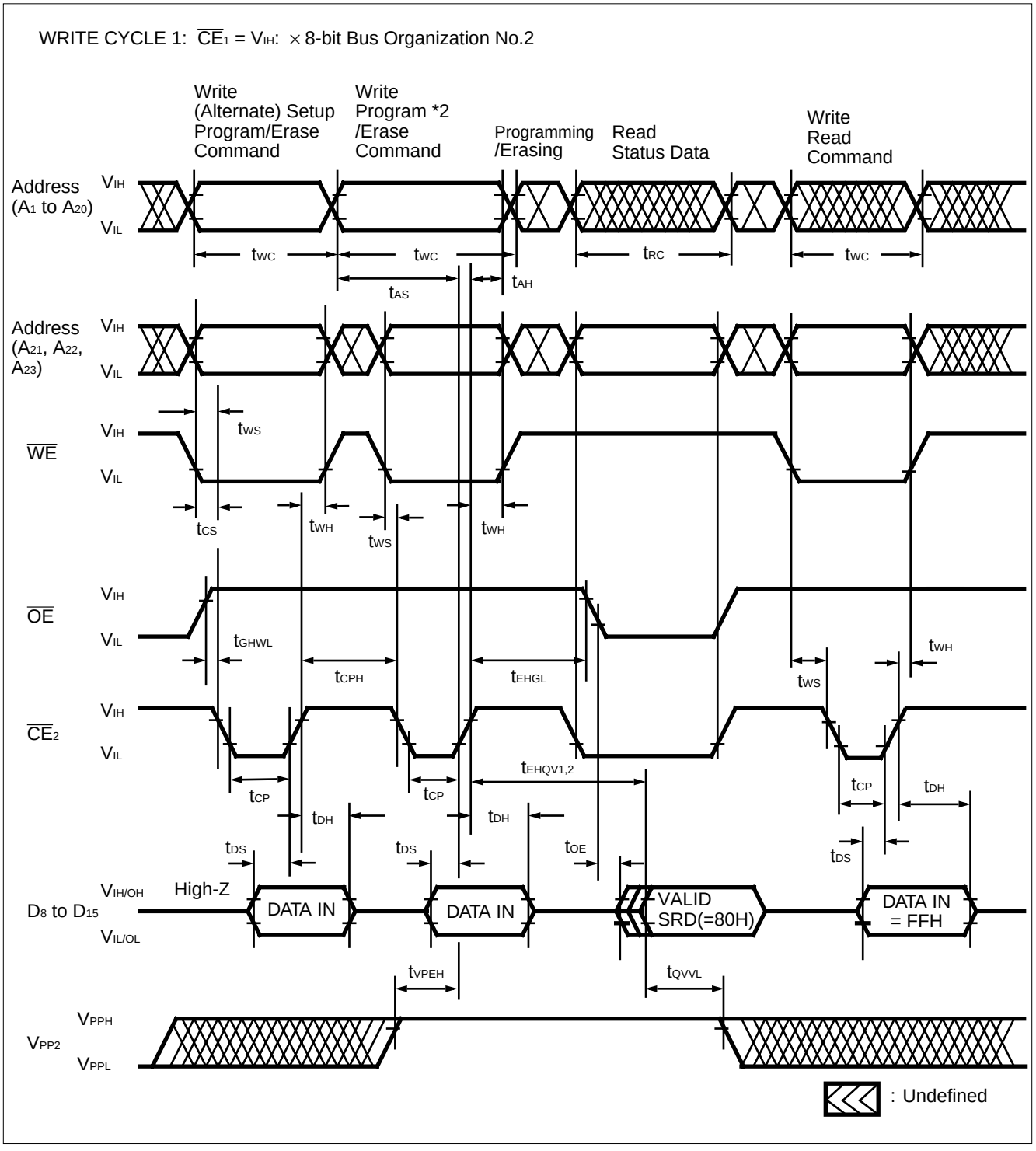
## MAIN MEMORY PROGRAM & ERASE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = $V_{IH}$) *1




**Notes:** *1. $A_0$, $A_{21}$, $A_{22}$ and $A_{23}$ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the PROGRAM/ERASE CHIP DECODING INFORMATION.

*2. Latch address and data.

## MAIN MEMORY PROGRAM & ERASE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = $V_{IH}$) *1

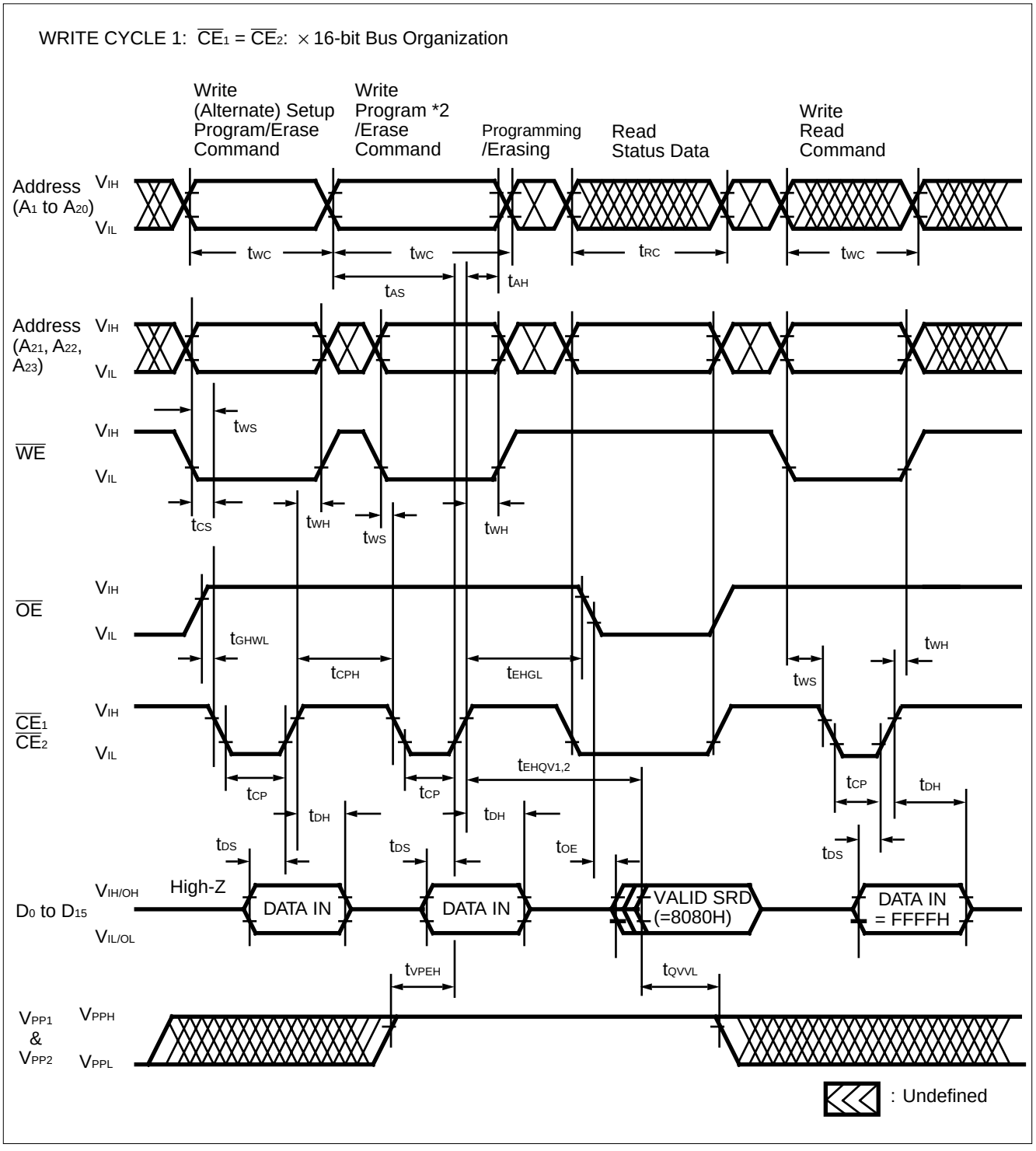



**Notes:** *1. $A_{21}$, $A_{22}$ and $A_{23}$ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the PROGRAM/ERASE CHIP DECODING INFORMATION. $A_0$ = $V_{IL}$ or $V_{IH}$.

*2. Latch address and data.

# MB98A8113x-/8123x-/8133x-/8143x-20

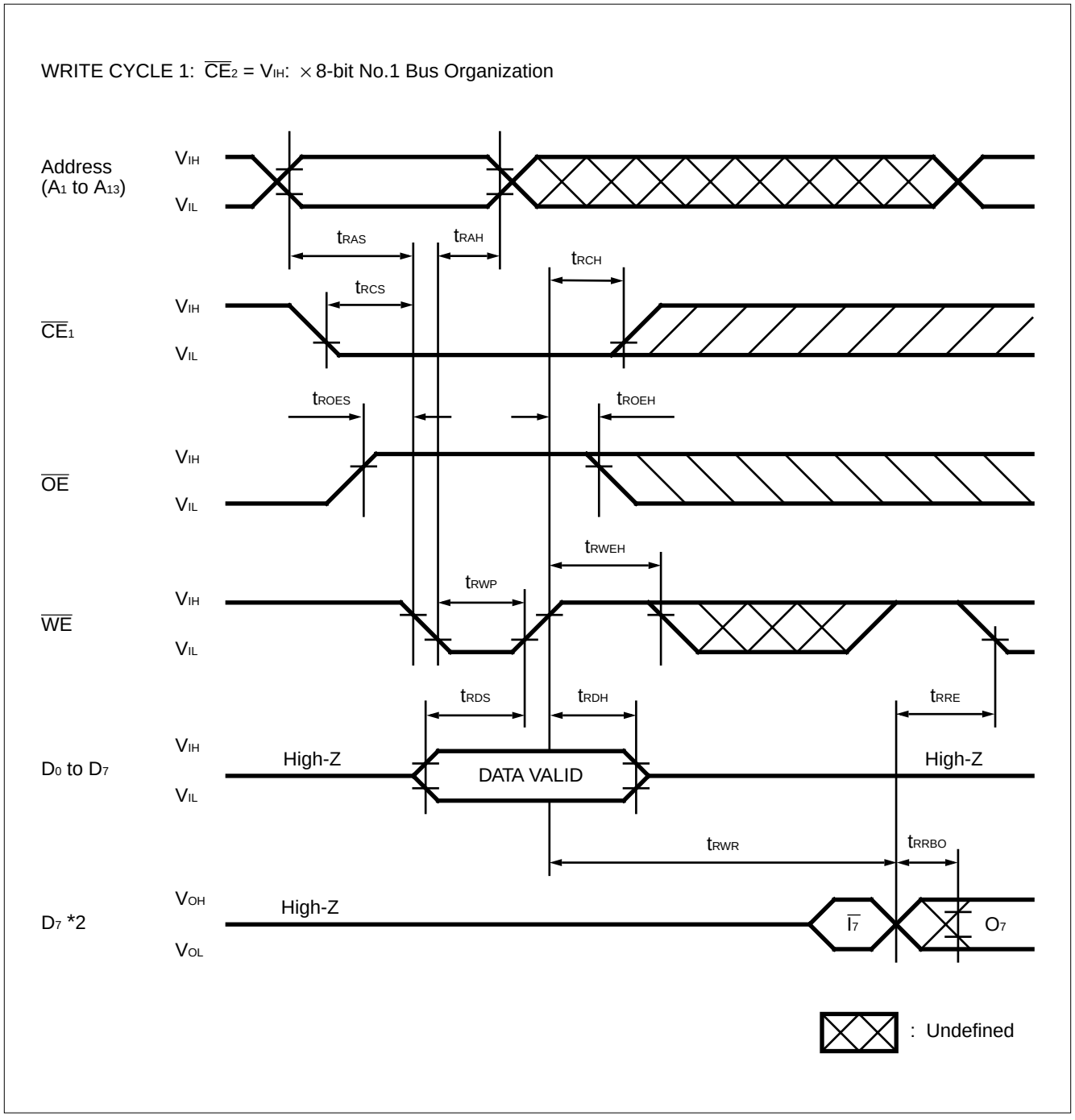
## MAIN MEMORY PROGRAM & ERASE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = $V_{IH}$) *1




**Notes:** *1. $A_{21}$, $A_{22}$ and $A_{23}$ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the PROGRAM/ERASE CHIP DECODING INFORMATION. $A_0$ = $V_{IL}$ or $V_{IH}$.

*2. Latch address and data.

## ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = $V_{IL}$) *1

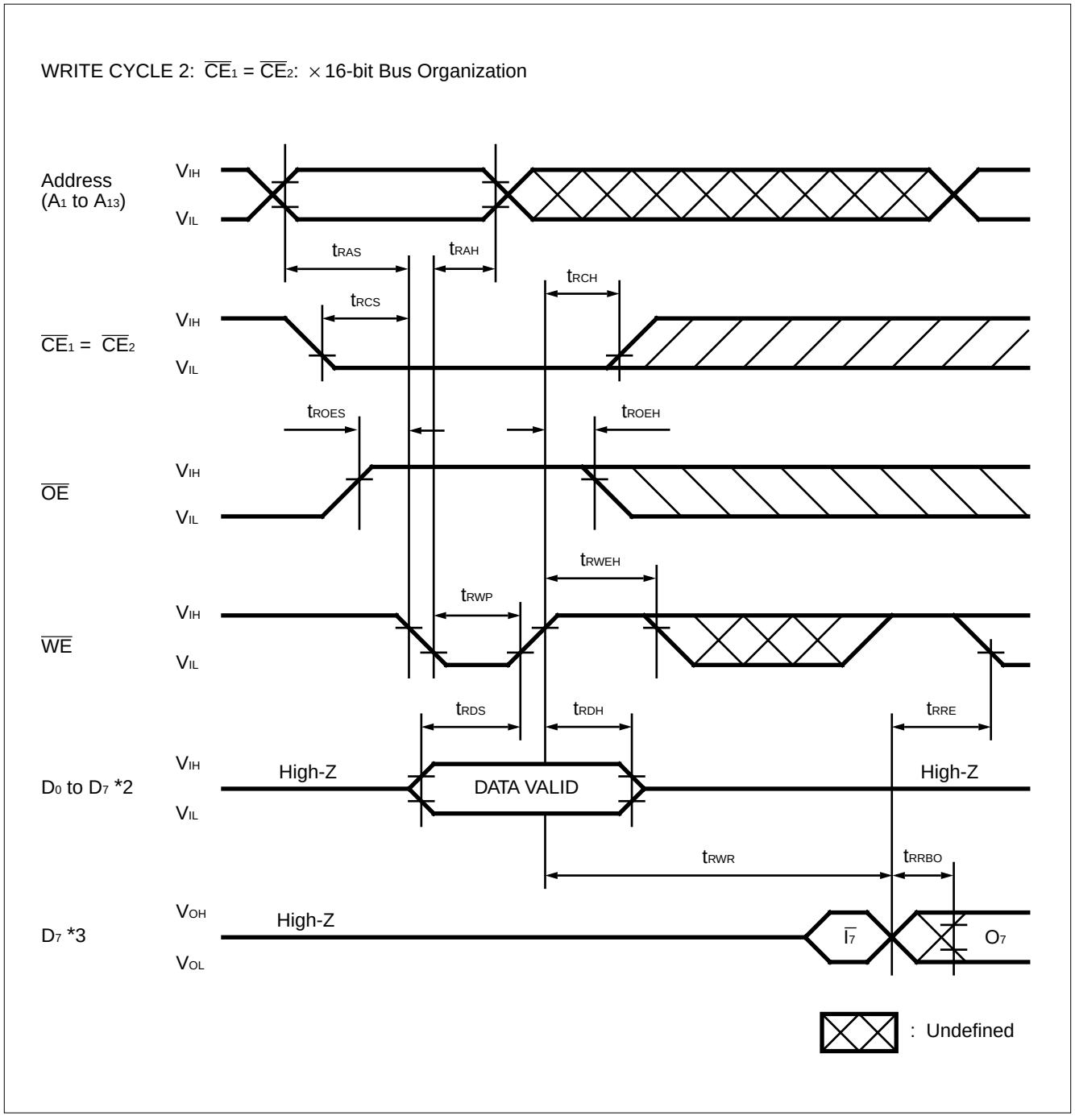



**Notes:** *1. This timing diagram is for MB98A81133, 81233, 81333, and 81433. “FF” data is available on MB98A81132, 81232, 81332, and 81432 only. $A_0$ = $V_{IL}$.

*2. Data polling operation.

# MB98A8113x-/8123x-/8133x-/8143x-20

## ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = $V_{IL}$) *1

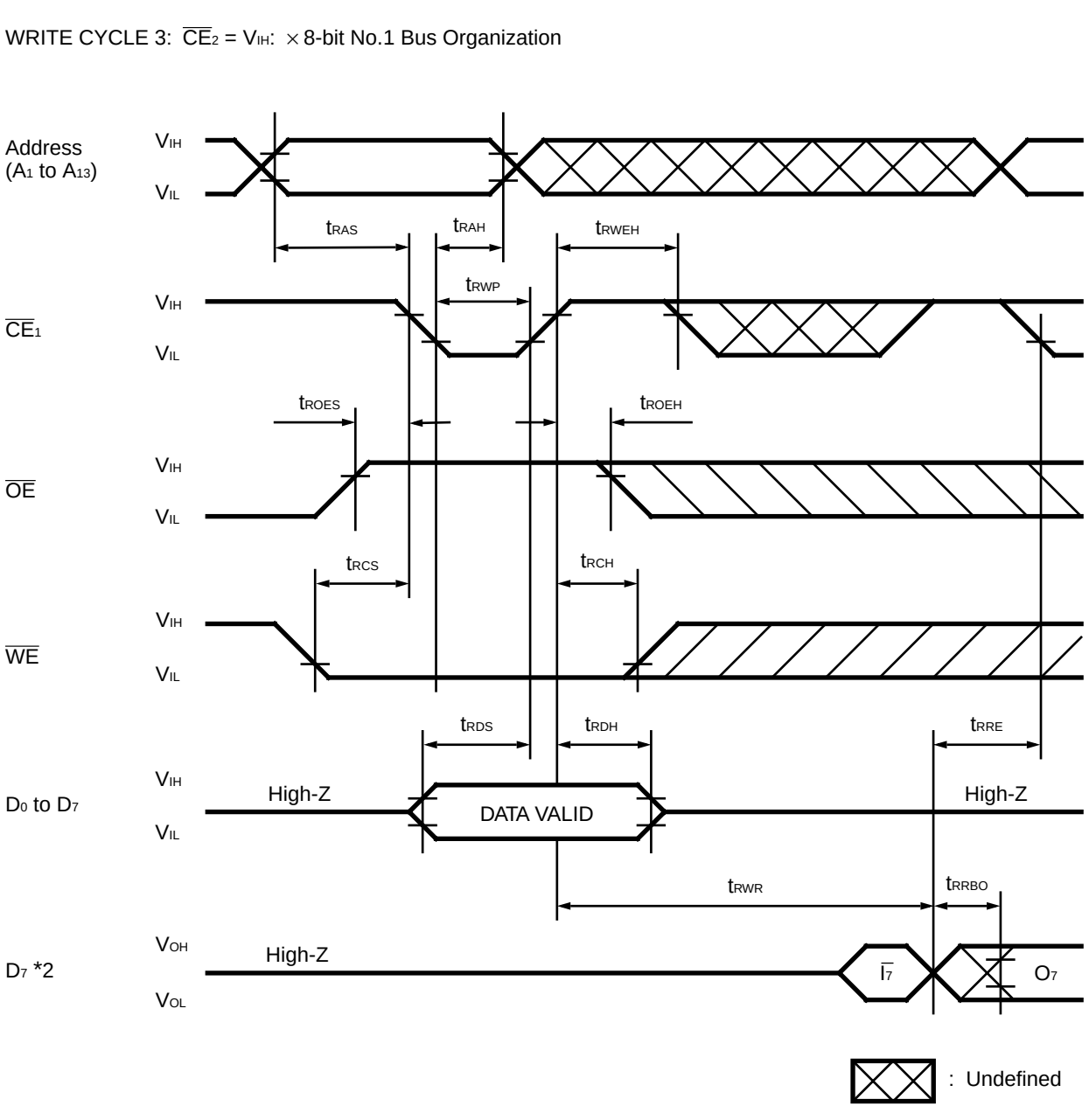



**Notes:** *1. This timing diagram is for MB98A81133, 81233, 81333, and 81433. “FF” data is available on MB98A81132, 81232, 81332, and 81432 only. $A_0$ = $V_{IH}$ or $V_{IL}$.

*2. Inputs from $D_8$ to $D_{15}$ are not defined.

*3. Data polling operation.

## ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = $V_{IL}$) *1

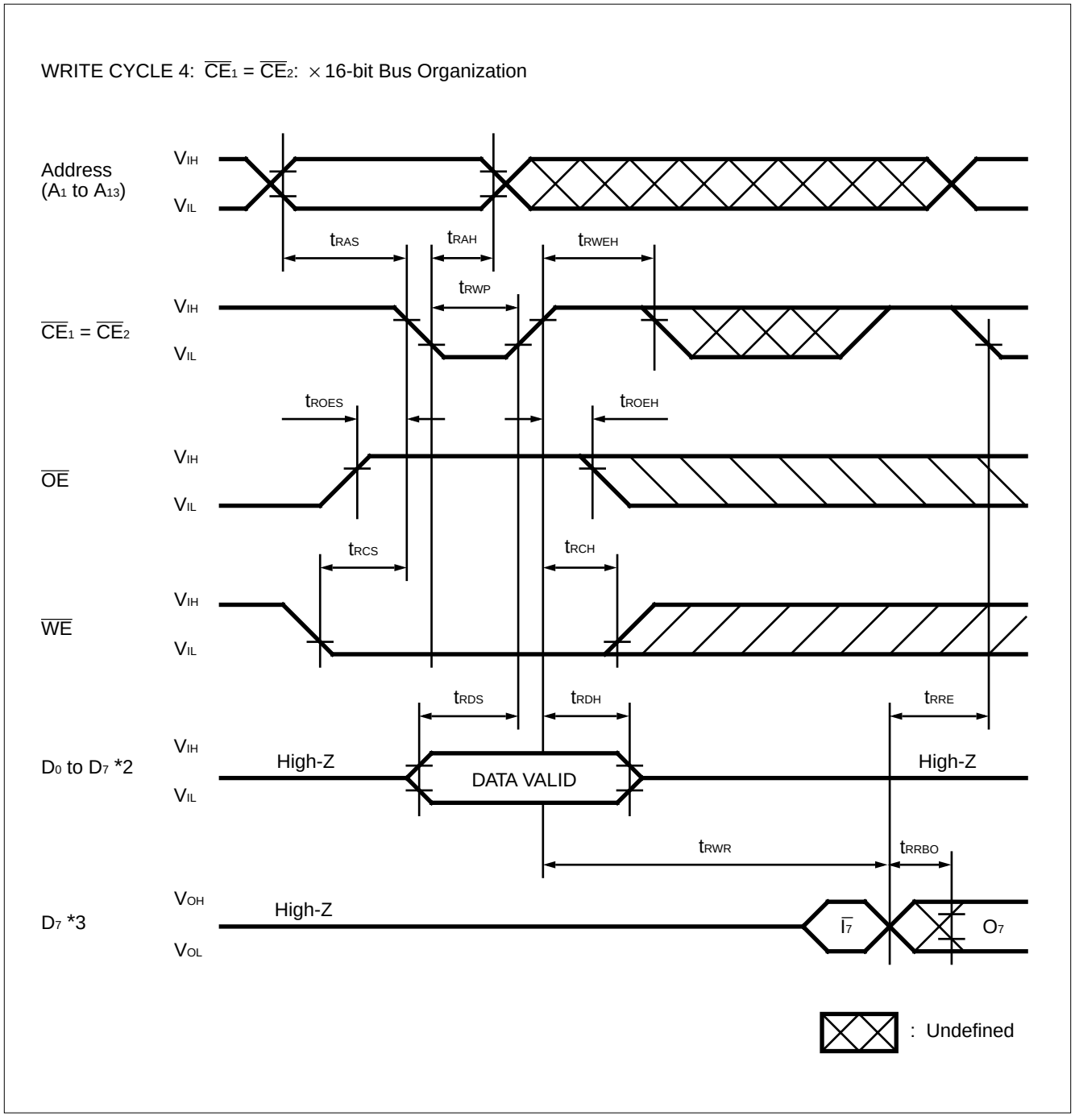



**Notes:** *1. This timing diagram is for MB98A81133, 81233, 81333 and 81433. $A_0$ = $V_{IL}$.

*2. Data polling operation.

# MB98A8113x-/8123x-/8133x-/8143x-20

## ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = $V_{IL}$) *1



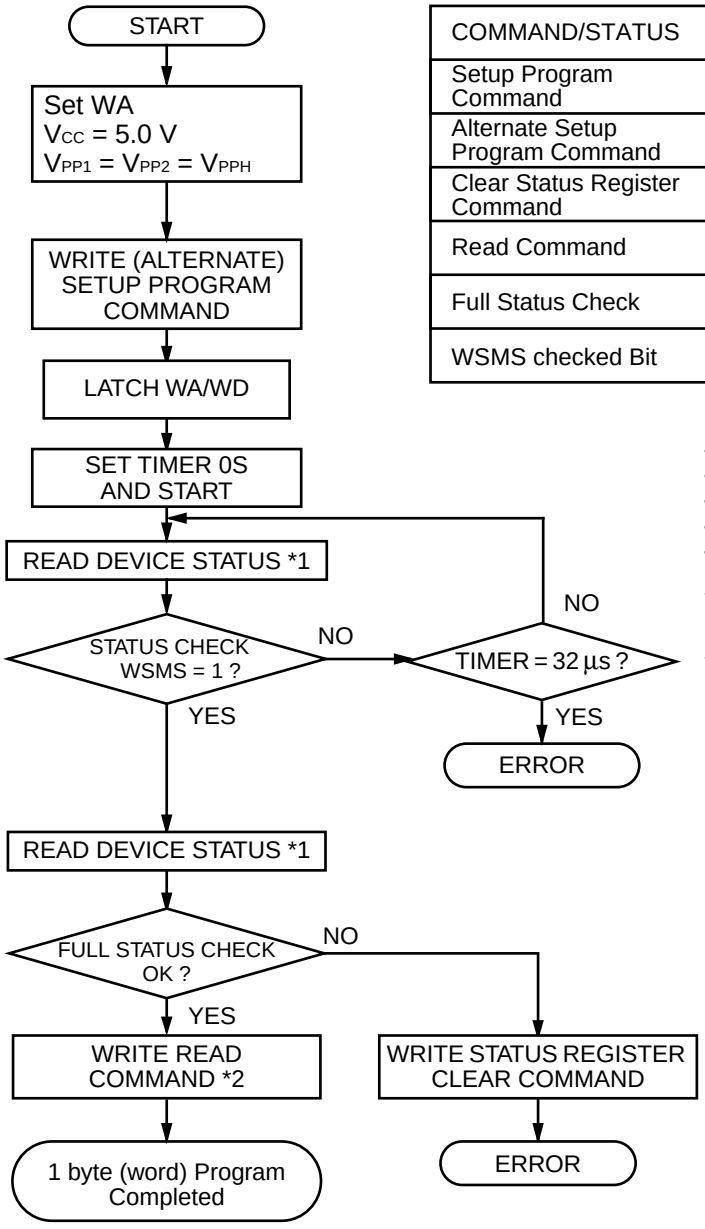

**Notes:** *1. This timing diagram is for MB98A81133, 81233, 81333, and 81433. $A_0$ = $V_{IL}$ or $V_{IH}$.

*2. Inputs from $D_8$ to $D_{15}$ are not defined.

*3. Data polling operation.

## ■ PROGRAM/ERASE INFORMATION

**Fig. 4 – PROGRAM FLOWCHART**




| COMMAND/STATUS | ×8 bit mode | ×16 bit mode |
|---|---|---|
| Setup Program Command | 40H | 4040H |
| Alternate Setup Program Command | 10H | 1010H |
| Clear Status Register Command | 50H | 5050H |
| Read Command | FFH | FFFFH |
| Full Status Check | 80H | 8080H |
| WSMS checked Bit | bit 7 | bit 7, 15 |

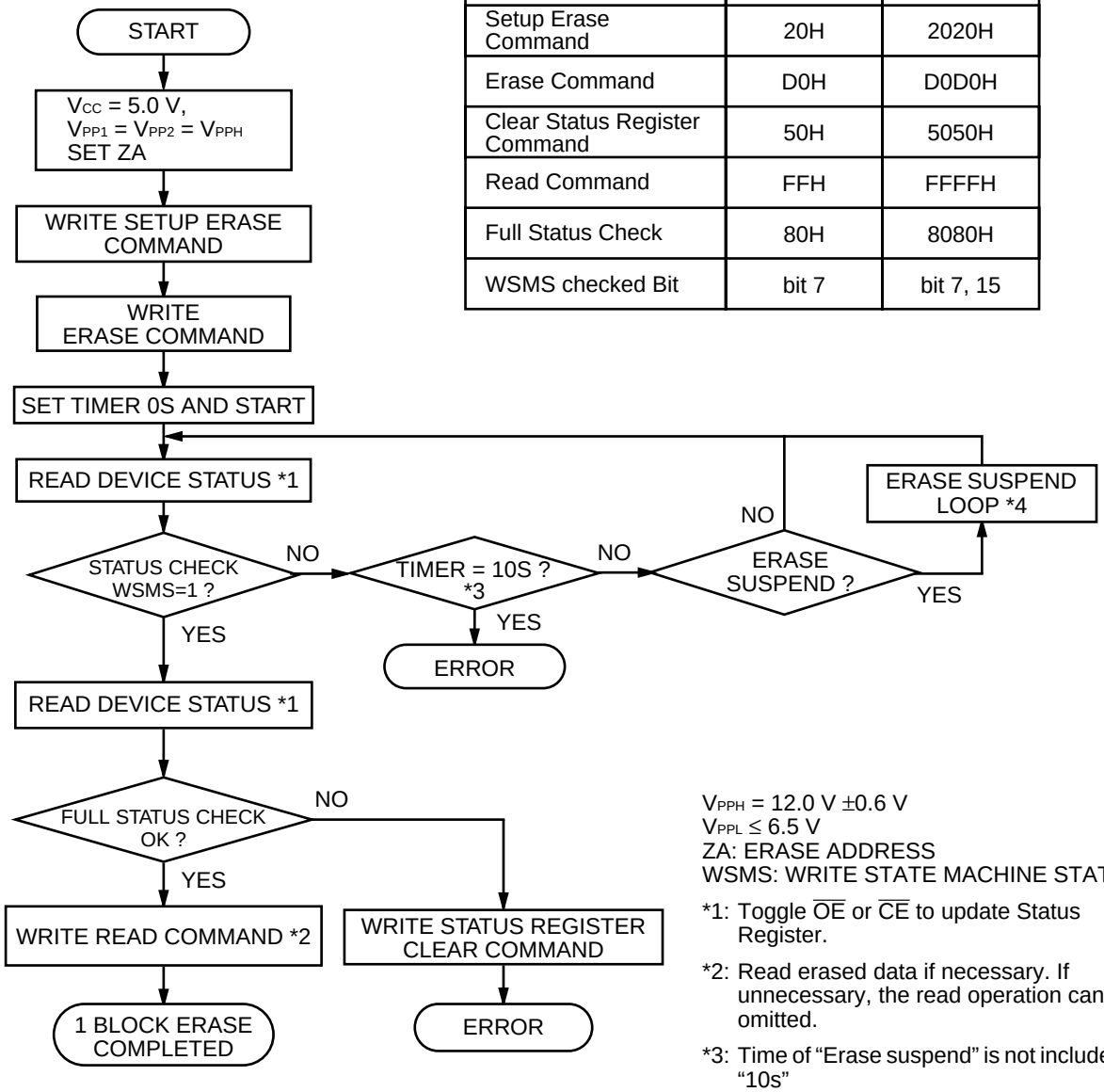
$V_{PPH}$ = 12.0 V ±0.6 V
$V_{PPL} \leq$ 6.5 V
WA: PROGRAMMING ADDRESS
WD: PROGRAMMING DATA
WSMS: WRITE STATE MACHINE STATUS

*1: Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register.

*2: Read programmed data if necessary. If unnecessary, the read operation can be omitted.

**Fig. 5 – ERASE FLOWCHART**

| COMMAND/STATUS | ×8 bit mode | ×16 bit mode |
|---|---|---|
| Setup Erase Command | 20H | 2020H |
| Erase Command | D0H | D0D0H |
| Clear Status Register Command | 50H | 5050H |
| Read Command | FFH | FFFFH |
| Full Status Check | 80H | 8080H |
| WSMS checked Bit | bit 7 | bit 7, 15 |




$V_{PPH}$ = 12.0 V ±0.6 V
$V_{PPL} \leq$ 6.5 V
ZA: ERASE ADDRESS
WSMS: WRITE STATE MACHINE STATUS

*1: Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register.

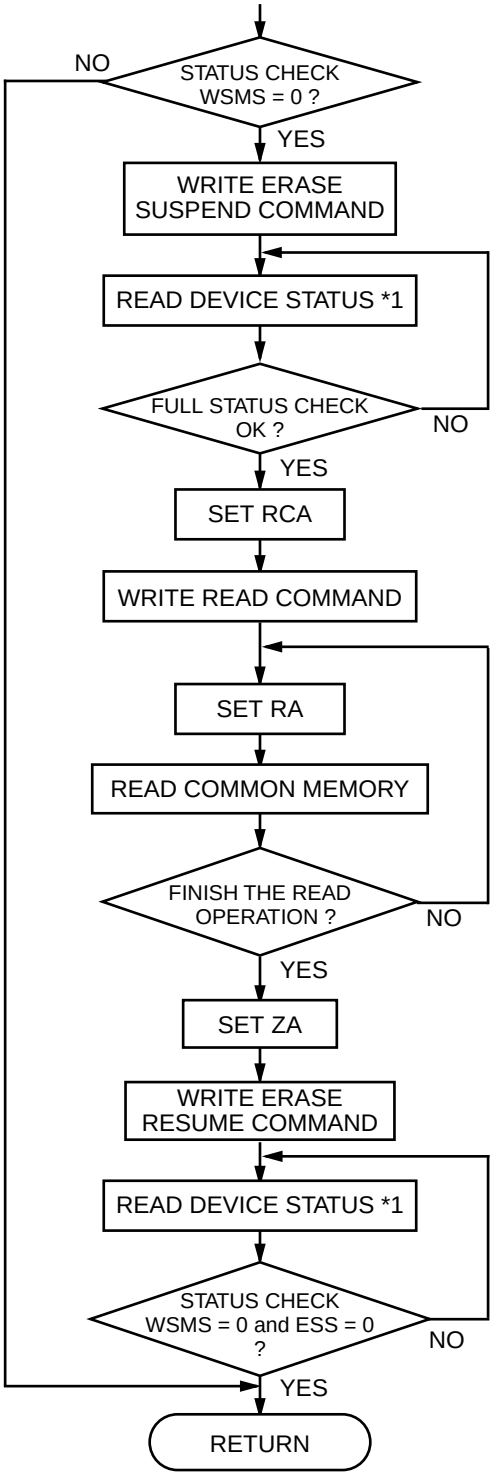
*2: Read erased data if necessary. If unnecessary, the read operation can be omitted.

*3: Time of “Erase suspend” is not included in “10s”

*4: Please see “Erase Suspend Loop” in next page.

**Note:** Erase both even and odd Address blocks at ×8 bit mode.

**Fig. 6 – ERASE SUSPEND LOOP**




| COMMAND/STATUS | ×8 bit mode | ×16 bit mode |
|---|---|---|
| Erase Suspend Command | B0H | B0B0H |
| Erase Resume Command | D0H | D0D0H |
| Read Command | FFH | FFFFH |
| Full Status Check | C0H | C0C0H |
| WSMS checked Bit | bit 7 | bit 7, 15 |
| ESS checked Bit | bit 6 | bit 6, 14 |

ZA: ERASE ADDRESS
WSMS: WRITE STATE MACHINE STATUS
ESS: ERASE SUSPEND STATUS
RCA: ADDRESS IN READ CHIP
RA: READ ADDRESS

*1: Toggle $\overline{OE}$ or $\overline{CE}$ to update Status Register.

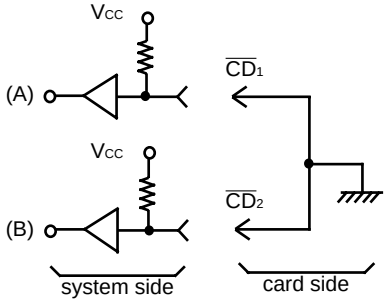
# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ UNIQUE FEATURES FOR FLASH MEMORY CARD

### 1. SPECIAL MONITORING PINS

#### 1.1 $\overline{CD_1}$, $\overline{CD_2}$: Card Detection Pins

$\overline{CD_1}$ and $\overline{CD_2}$ are to detect whether or not the card has been correctly inserted. (See Fig. 7.)
When the memory card has been correctly inserted, $\overline{CD_1}$ and $\overline{CD_2}$ are detected by the system. $\overline{CD_1}$, $\overline{CD_2}$ are tied to ground on the card side as shown in Fig. 7.



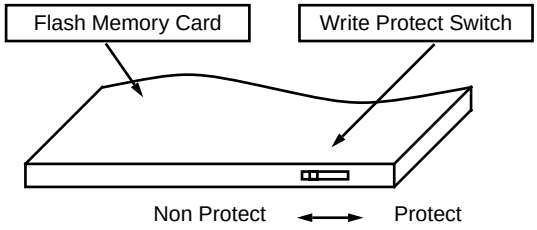

**– Fig. 7 –**

#### 1.2 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 8, the Flash memory card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the "Non Protect" position and the $\overline{WE}$ pin low. And at that time, L-level is output on the WP pin.

To prevent writing to the card, the switch must be turned to the "Protect" position. At that time, H-level is output on the WP pin.




**– Fig. 8 –**

| WP Switch | WP (output) |
|---|---|
| Protect | H |
| Non Protect | L |

## ■ DEVICE HANDLING PRECAUTIONS

This device in composed of fine electronic parts, so take care in handling or keeping it as below.

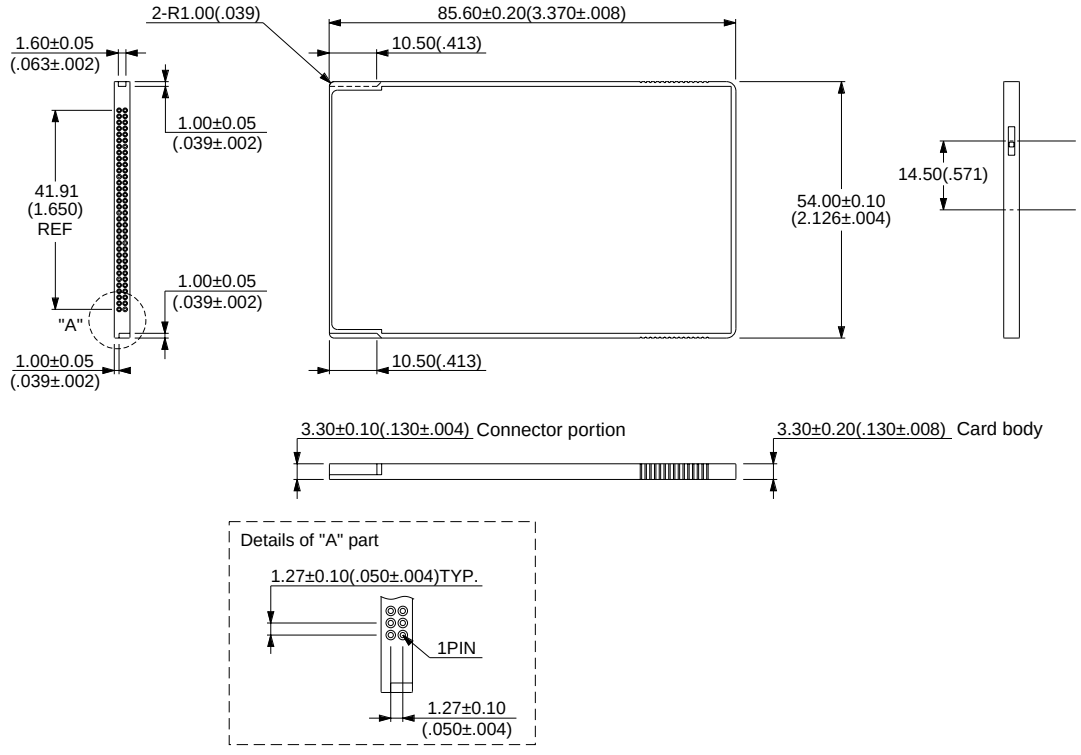
- The card is made fine,so do not keep it in the high temperature nor high humiditly, place like in the direct sunshine nor near the heater.
- The card shoud not be bent, scratched, dropped nor be shocked violently.
- This device shoud never be taken a part. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.

# MB98A8113x-/8123x-/8133x-/8143x-20

## ■ PACKAGE DIMENSIONS

68-PIN MEMORY CARD
(CRD-68P-M05)

Note: Dimensions conform with "PC Card Standard 95"




Dimensions in mm (inches)

# MB98A8113x-/8123x-/8133x-/8143x-20

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